GigaDevice Semiconductor Inc.

GD32E103xx
Arm® Cortex®-M4 32-bit MCU

Datasheet

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1. General description

The GD32E103xx device belongs to the connectivity line of GD32 MCU Family. It is a 32-bit general-purpose microcontroller based on the Arm® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides powerful trace technology for enhanced application security and advanced debug support.

The GD32E103xx device incorporates the Arm® Cortex®-M4 32-bit processor core operating at 120 MHz frequency with Flash accesses to obtain maximum efficiency. It provides up to 128 KB on-chip Flash memory and 32 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to two 12-bit 3 MSPS ADCs, two 12-bit DACs, up to ten general 16-bit timers, two 16-bit PWM advanced timers, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to three SPIs, two I2Cs, three USARTs and two UARTs, two I2Ss and an USBFS.

The device operates from 1.71 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make GD32E103xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, motor drives, consumer and handheld equipment, human machine interface, security and alarm systems, POS, automotive navigation, IoT and so on.

2. Device overview

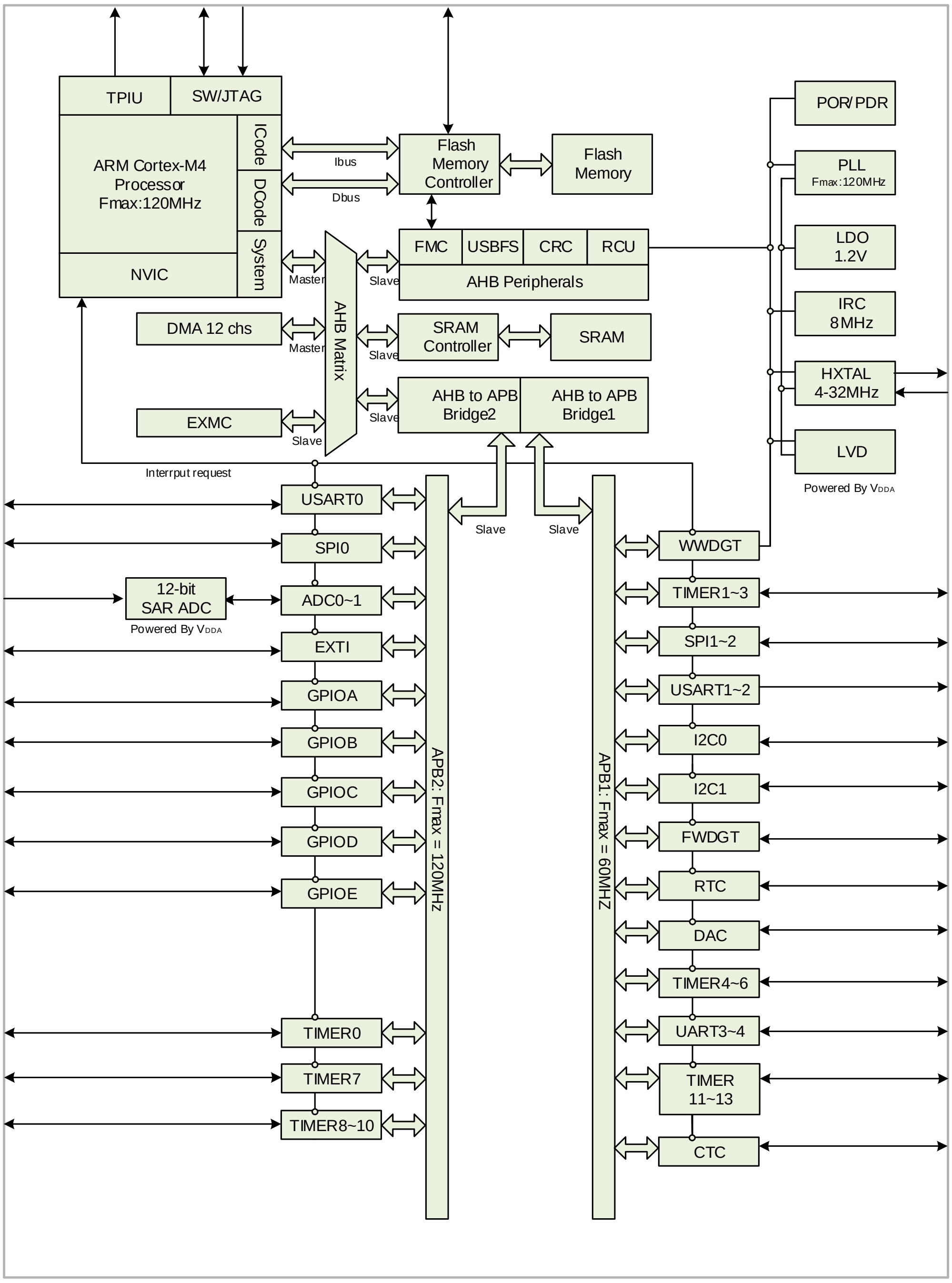
2.1. Device information

Table 2-1. GD32E103xx devices features and peripheral list

Part Number		GD32E103xx							
		T8	TB	C8	CB	R8	RB	V8	VB
Flash (KB)		64	128	64	128	64	128	64	128
SRAM (KB)		20	32	20	32	20	32	20	32
Timers	General timer(16-bit)	4 (1-4)	4 (1-4)	10 (1-4,8-13)	10 (1-4,8-13)	10 (1-4,8-13)	10 (1-4,8-13)	10 (1-4,8-13)	10 (1-4,8-13)
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)
	SysTick	1	1	1	1	1	1	1	1
	Basic timer(16-bit)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)
	Watchdog	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1
Connectivity	USART	2 (0-1)	2 (0-1)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)
	UART	0	0	0	0	2 (3-4)	2 (3-4)	2 (3-4)	2 (3-4)
	I2C	1 (0)	1 (0)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	SPI/I2S	1/0 (0/-)	1/0 (0/-)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)
	USBFS	1	1	1	1	1	1	1	1
GPIO		26	26	37	37	51	51	80	80
EXMC		0	0	0	0	0	0	1	1
EXTI		16	16	16	16	16	16	16	16
ADC	Units	2	2	2	2	2	2	2	2
	Channels	10	10	10	10	16	16	16	16
DAC		2	2	2	2	2	2	2	2
Package		QFN36		LQFP48		LQFP64		LQFP100	

2.2. Block diagram

Figure 2-1.GD32E103xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32E103Vx LQFP100 pinouts

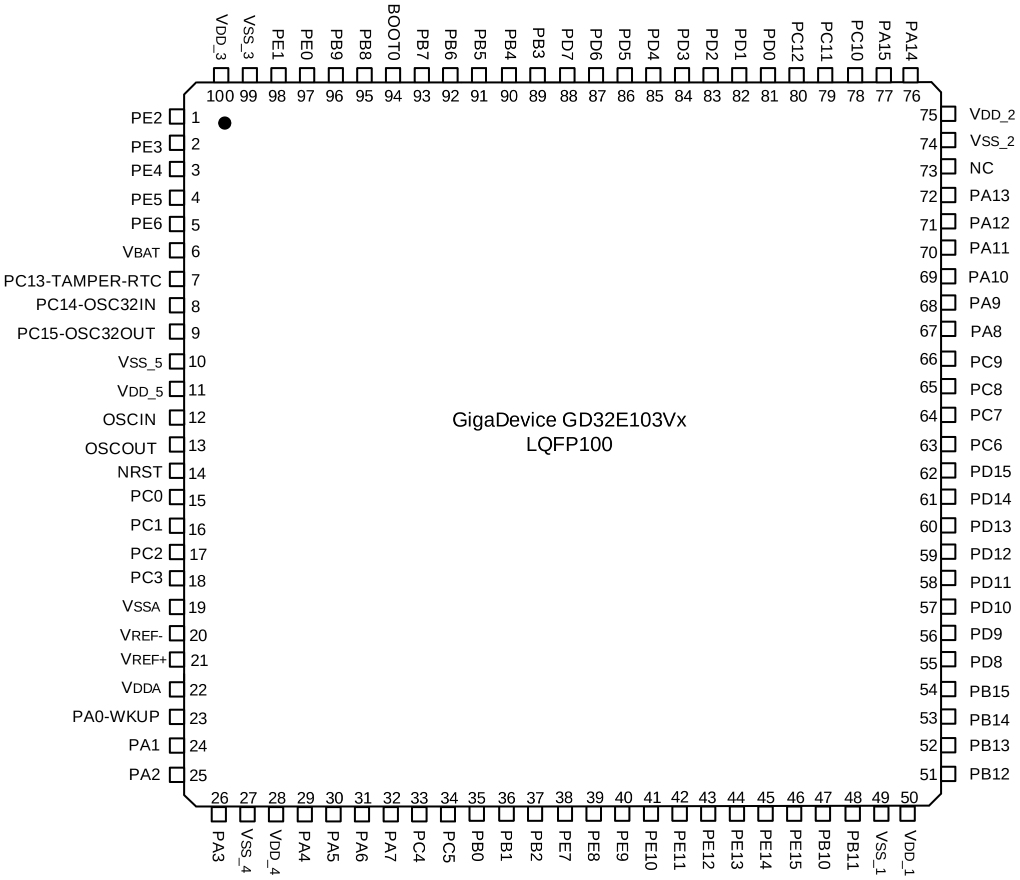


Figure 2-3. GD32E103Rx LQFP64 pinouts

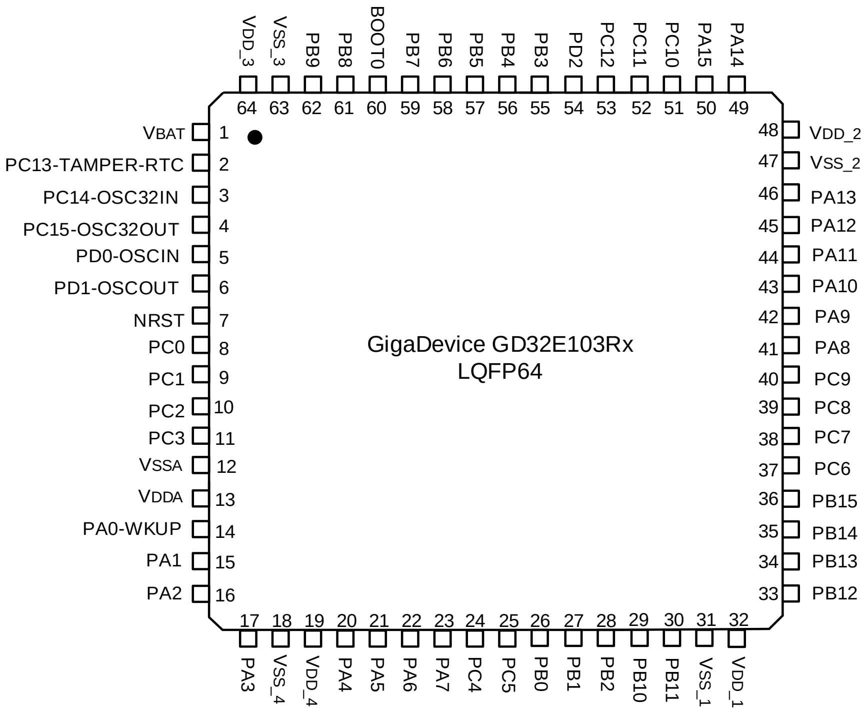


Figure 2-4. GD32E103Cx LQFP48 pinouts

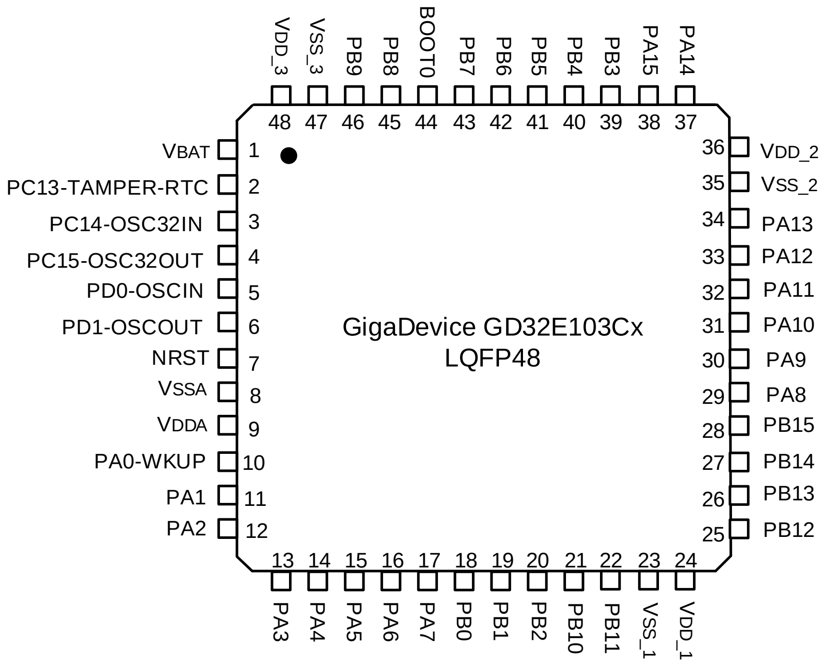
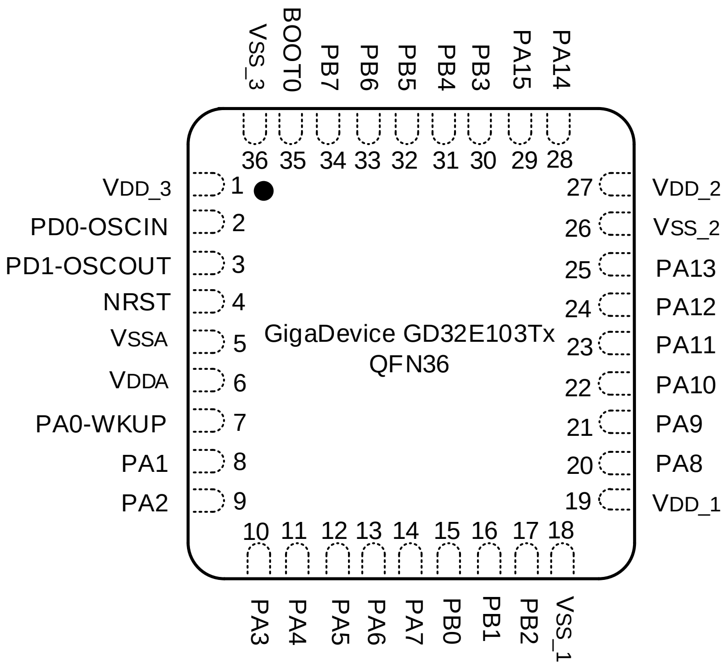


Figure 2-5. GD32E103Tx QFN36 pinouts



2.4. Memory map

Table 2-2. GD32E103xx memory map

Pre-defined regions	Bus	Address	Peripherals
External device	AHB3	0xA000 0000 - 0xA000 0FFF	EXMC - SWREG
External RAM		0x9000 0000 - 0x9FFF FFFF	Reserved
		0x7000 0000 - 0x8FFF FFFF	Reserved
		0x6000 0000 - 0x63FF FFFF	EXMC - NOR/PSRAM/SRAM
Peripheral	AHB1	0x5000 0000 - 0x5003 FFFF	USBFS
		0x4008 0000 - 0x4FFF FFFF	Reserved
		0x4004 0000 - 0x4007 FFFF	Reserved
		0x4002 BC00 - 0x4003 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	Reserved
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	Reserved
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	Reserved
		0x4002 6000 - 0x4002 63FF	Reserved
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	Reserved
		0x4002 3C00 - 0x4002 3FFF	Reserved

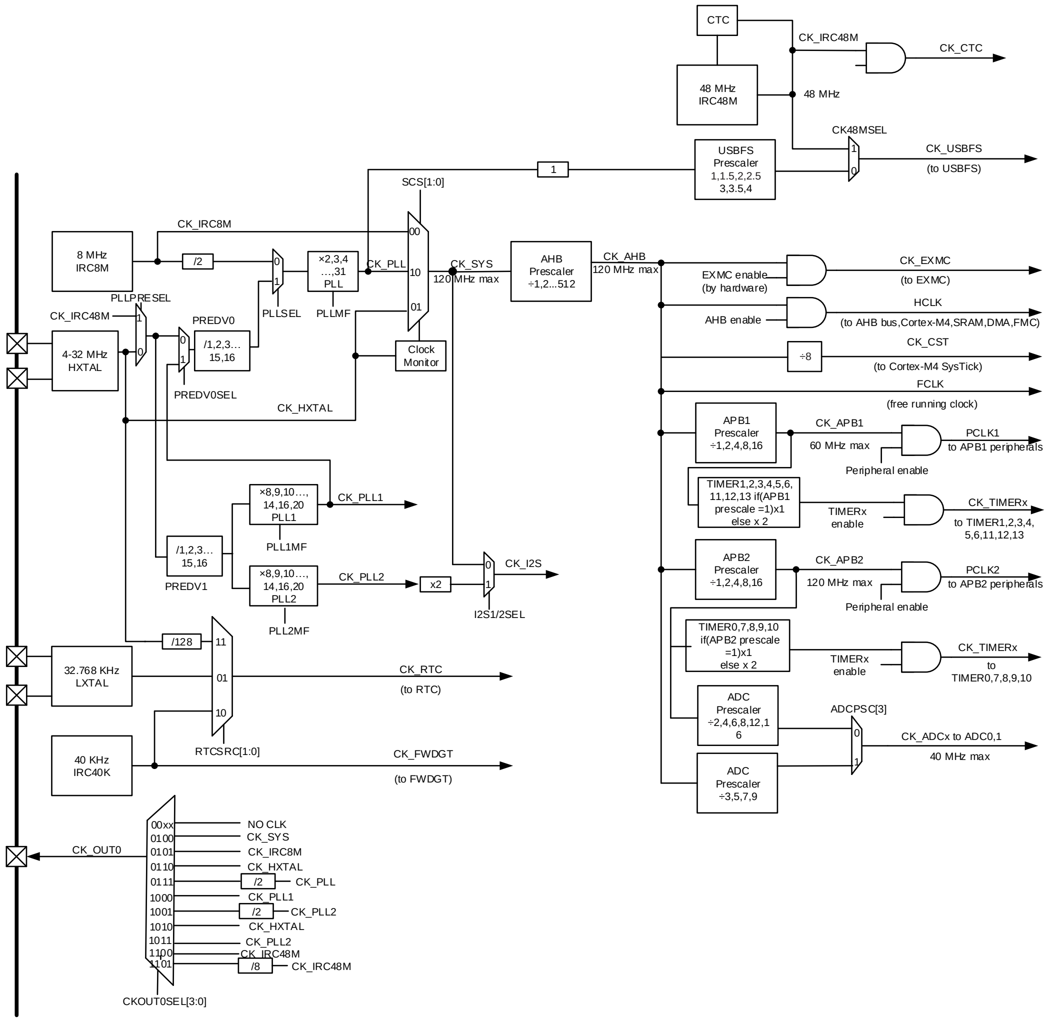
Pre-defined regions	Bus	Address	Peripherals
		0x4002 3800 - 0x4002 3BFF	Reserved
		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	Reserved
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	Reserved
		0x4002 0400 - 0x4002 07FF	DMA1
		0x4002 0000 - 0x4002 03FF	DMA0
		0x4001 8400 - 0x4001 FFFF	Reserved
		0x4001 8000 - 0x4001 83FF	Reserved
	APB2	0x4001 7C00 - 0x4001 7FFF	Reserved
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	Reserved
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 5C00 - 0x4001 67FF	Reserved
		0x4001 5800 - 0x4001 5BFF	Reserved
		0x4001 5400 - 0x4001 57FF	TIMER10
		0x4001 5000 - 0x4001 53FF	TIMER9
		0x4001 4C00 - 0x4001 4FFF	TIMER8
		0x4001 4800 - 0x4001 4BFF	Reserved
		0x4001 4400 - 0x4001 47FF	Reserved
		0x4001 4000 - 0x4001 43FF	Reserved
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	TIMER7
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	ADC1
		0x4001 2400 - 0x4001 27FF	ADC0
		0x4001 2000 - 0x4001 23FF	Reserved

Pre-defined regions	Bus	Address	Peripherals
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	GPIOE
		0x4001 1400 - 0x4001 17FF	GPIOD
		0x4001 1000 - 0x4001 13FF	GPIOC
		0x4001 0C00 - 0x4001 0FFF	GPIOB
		0x4001 0800 - 0x4001 0BFF	GPIOA
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	AFIO
	APB1	0x4000 CC00 - 0x4000 FFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	CTC
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	DAC
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	BKP
		0x4000 6800 - 0x4000 6BFF	Reserved
		0x4000 6400 - 0x4000 67FF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1C00 - 0x4000 1FFF	TIMER12
		0x4000 1800 - 0x4000 1BFF	TIMER11

Pre-defined regions	Bus	Address	Peripherals
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB	0x2007 0000 - 0x3FFF FFFF	Reserved
		0x2006 0000 - 0x2006 FFFF	Reserved
		0x2003 0000 - 0x2005 FFFF	Reserved
		0x2002 0000 - 0x2002 FFFF	Reserved
		0x2001 C000 - 0x2001 FFFF	SRAM
		0x2001 8000 - 0x2001 BFFF	
		0x2000 5000 - 0x2001 7FFF	
		0x2000 0000 - 0x2000 4FFF	
Code	AHB	0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option Bytes
		0x1FFF F000 - 0x1FFF F7FF	Boot loader
		0x1FFF C010 - 0x1FFF EFFF	
		0x1FFF C000 - 0x1FFF C00F	
		0x1FFF B000 - 0x1FFF BFFF	
		0x1FFF 7A10 - 0x1FFF AFFF	Reserved
		0x1FFF 7800 - 0x1FFF 7A0F	Reserved
		0x1FFF 0000 - 0x1FFF 77FF	Reserved
		0x1FFE C010 - 0x1FFE FFFF	Reserved
		0x1FFE C000 - 0x1FFE C00F	Reserved
		0x1001 0000 - 0x1FFE BFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	Reserved
		0x083C 0000 - 0x0FFF FFFF	Reserved
		0x0830 0000 - 0x083B FFFF	Reserved
		0x0810 0000 - 0x082F FFFF	Main Flash
		0x0802 0000 - 0x080F FFFF	
		0x0800 0000 - 0x0801 FFFF	
		0x0030 0000 - 0x07FF FFFF	Reserved
		0x0010 0000 - 0x002F FFFF	Aliased to Main Flash or Boot loader
		0x0002 0000 - 0x000F FFFF	
		0x0000 0000 - 0x0001 FFFF	

2.5. Clock tree

Figure 2-6. GD32E103xx clock tree



Legend:

HXTAL: 4 to 32 MHz High Speed crystal oscillator

LXTAL: 32,768 Hz Low Speed crystal oscillator

IRC8M: Internal 8 MHz RC oscillator

IRC40K: Internal 40 KHz RC oscillator

IRC48M: Internal 48 MHz RC oscillator

2.6. Pin definitions

Notes:

For GD32E103Rx LQFP64、GD32E103Cx LQFP48 and GD32E103Tx QFN36, V_{REF-} and V_{REF+} are internally connected to V_{SSA} and V_{DDA} respectively.

2.6.1. GD32E103Vx LQFP100 pin definitions

Table 2-3. GD32E103Vx LQFP100 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PE2	1	I/O	5VT	Default: PE2 Alternate: EXMC_A23
PE3	2	I/O	5VT	Default: PE3 Alternate: EXMC_A19
PE4	3	I/O	5VT	Default: PE4 Alternate: EXMC_A20
PE5	4	I/O	5VT	Default: PE5 Alternate: EXMC_A21 Remap: TIMER8_CH0
PE6	5	I/O	5VT	Default: PE6 Alternate: EXMC_A22 Remap: TIMER8_CH1
V_{BAT}	6	P	-	Default: V_{BAT}
PC13-TAMPER-RTC	7	I/O	-	Default: PC13 Alternate: RTC_TAMPER
PC14-OSC32IN	8	I/O	-	Default: PC14 Alternate: OSC32IN
PC15-OSC32OUT	9	I/O	-	Default: PC15 Alternate: OSC32OUT
V_{SS_5}	10	P	-	Default: V_{SS_5}
V_{DD_5}	11	P	-	Default: V_{DD_5}
OSCIN	12	I	-	Default: OSCIN Remap: PD0
OSCOUT	13	O	-	Default: OSCOUT Remap:PD1
NRST	14	I/O	-	Default: NRST
PC0	15	I/O	-	Default: PC0 Alternate: ADC01_IN10
PC1	16	I/O	-	Default: PC1 Alternate: ADC01_IN11
PC2	17	I/O	-	Default: PC2 Alternate: ADC01_IN12
PC3	18	I/O	-	Default: PC3 Alternate: ADC01_IN13
V_{SSA}	19	P	-	Default: V_{SSA}
V_{REF-}	20	P	-	Default: V_{REF-}

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{REF+}	21	P	-	Default: V_{REF+}
V_{DDA}	22	P	-	Default: V_{DDA}
PA0-WKUP	23	I/O	-	Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI
PA1	24	I/O	-	Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1, TIMER1_CH1
PA2	25	I/O	-	Default: PA2 Alternate: USART1_TX, TIMER4_CH2, ADC01_IN2, TIMER8_CH0, TIMER1_CH2, SPI0_IO2
PA3	26	I/O	-	Default: PA3 Alternate: USART1_RX, TIMER4_CH3, ADC01_IN3, TIMER1_CH3, TIMER8_CH1, SPI0_IO3
V_{SS_4}	27	P	-	Default: V_{SS_4}
V_{DD_4}	28	P	-	Default: V_{DD_4}
PA4	29	I/O	-	Default: PA4 Alternate: SPI0_NSS, USART1_CK, DAC_OUT0, ADC01_IN4 Remap: SPI2_NSS, I2S2_WS
PA5	30	I/O	-	Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1
PA6	31	I/O	-	Default: PA6 Alternate: SPI0_MISO, TIMER7_BRKIN, ADC01_IN6, TIMER2_CH0, TIMER12_CH0 Remap: TIMER0_BRKIN
PA7	32	I/O	-	Default: PA7 Alternate: SPI0_MOSI, TIMER7_CH0_ON, ADC01_IN7, TIMER2_CH1, TIMER13_CH0 Remap: TIMER0_CH0_ON
PC4	33	I/O	-	Default: PC4 Alternate: ADC01_IN14
PC5	34	I/O	-	Default: PC5 Alternate: ADC01_IN15
PB0	35	I/O	-	Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON Remap: TIMER0_CH1_ON
PB1	36	I/O	-	Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON Remap: TIMER0_CH2_ON
PB2	37	I/O	5VT	Default: PB2, BOOT1

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PE7	38	I/O	5VT	Default: PE7 Alternate: EXMC_D4 Remap: TIMER0_ETI
PE8	39	I/O	5VT	Default: PE8 Alternate: EXMC_D5 Remap: TIMER0_CH0_ON
PE9	40	I/O	5VT	Default: PE9 Alternate: EXMC_D6 Remap: TIMER0_CH0
PE10	41	I/O	5VT	Default: PE10 Alternate: EXMC_D7 Remap: TIMER0_CH1_ON
PE11	42	I/O	5VT	Default: PE11 Alternate: EXMC_D8 Remap: TIMER0_CH1
PE12	43	I/O	5VT	Default: PE12 Alternate: EXMC_D9 Remap: TIMER0_CH2_ON
PE13	44	I/O	5VT	Default: PE13 Alternate: EXMC_D10 Remap: TIMER0_CH2
PE14	45	I/O	5VT	Default: PE14 Alternate: EXMC_D11 Remap: TIMER0_CH3
PE15	46	I/O	5VT	Default: PE15 Alternate: EXMC_D12 Remap: TIMER0_BRKIN
PB10	47	I/O	5VT	Default: PB10 Alternate: I2C1_SCL, USART2_TX Remap: TIMER1_CH2
PB11	48	I/O	5VT	Default: PB11 Alternate: I2C1_SDA, USART2_RX Remap: TIMER1_CH3
V_{SS_1}	49	P	-	Default: V_{SS_1}
V_{DD_1}	50	P	-	Default: V_{DD_1}
PB12	51	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2S1_WS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN
PB13	52	I/O	5VT	Default: PB13 Alternate: SPI1_SCK, I2S1_CK, USART2_CTS, TIMER0_CH0_ON, I2C1_TXFRAME

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB14	53	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0
PB15	54	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER0_CH2_ON, TIMER11_CH1
PD8	55	I/O	5VT	Default: PD8 Alternate: EXMC_D13 Remap: USART2_TX
PD9	56	I/O	5VT	Default: PD9 Alternate: EXMC_D14 Remap: USART2_RX
PD10	57	I/O	5VT	Default: PD10 Alternate: EXMC_D15 Remap: USART2_CK
PD11	58	I/O	5VT	Default: PD11 Alternate: EXMC_A16 Remap: USART2_CTS
PD12	59	I/O	5VT	Default: PD12 Alternate: EXMC_A17 Remap: TIMER3_CH0, USART2_RTS
PD13	60	I/O	5VT	Default: PD13 Alternate: EXMC_A18 Remap: TIMER3_CH1
PD14	61	I/O	5VT	Default: PD14 Alternate: EXMC_D0 Remap: TIMER3_CH2
PD15	62	I/O	5VT	Default: PD15 Alternate: EXMC_D1 Remap: TIMER3_CH3, CTC_SYNC
PC6	63	I/O	5VT	Default: PC6 Alternate: I2S1_MCK, TIMER7_CH0 Remap: TIMER2_CH0
PC7	64	I/O	5VT	Default: PC7 Alternate: I2S2_MCK, TIMER7_CH1 Remap: TIMER2_CH1
PC8	65	I/O	5VT	Default: PC8 Alternate: TIMER7_CH2 Remap: TIMER2_CH2

Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
PC9	66	I/O	5VT	Default: PC9 Alternate: TIMER7_CH3 Remap: TIMER2_CH3
PA8	67	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, VCORE, USBFS_SOF, CTC_SYNC
PA9	68	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS
PA10	69	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, USBFS_ID, V1REF
PA11	70	I/O	5VT	Default: PA11 Alternate: USART0_CTS, USBFS_DM, TIMER0_CH3
PA12	71	I/O	5VT	Default: PA12 Alternate: USART0_RTS, USBFS_DP, TIMER0_ETI
PA13	72	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
NC	73	-	-	-
V_{SS_2}	74	P	-	Default: V_{SS_2}
V_{DD_2}	75	P	-	Default: V_{DD_2}
PA14	76	I/O	5VT	Default: JTCK, SWCLK Remap:PA14
PA15	77	I/O	5VT	Default: JTDI Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS
PC10	78	I/O	5VT	Default: PC10 Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK
PC11	79	I/O	5VT	Default: PC11 Alternate: UART3_RX Remap: USART2_RX, SPI2_MISO
PC12	80	I/O	5VT	Default: PC12 Alternate: UART4_TX Remap: USART2_CK, SPI2_MOSI, I2S2_SD
PD0	81	I/O	5VT	Default: PD0 Alternate: EXMC_D2 Remap: OSCIN
PD1	82	I/O	5VT	Default: PD1 Alternate: EXMC_D3 Remap: OSCOUT
PD2	83	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PD3	84	I/O	5VT	Default: PD3 Alternate: EXMC_CLK Remap: USART1_CTS
PD4	85	I/O	5VT	Default: PD4 Alternate: EXMC_NOE Remap: USART1_RTS
PD5	86	I/O	5VT	Default: PD5 Alternate: EXMC_NWE Remap: USART1_TX
PD6	87	I/O	5VT	Default: PD6 Alternate: EXMC_NWAIT Remap: USART1_RX
PD7	88	I/O	5VT	Default: PD7 Alternate: EXMC_NE0 Remap: USART1_CK
PB3	89	I/O	5VT	Default: JTDO Alternate: SPI2_SCK, I2S2_CK Remap: TIMER1_CH1, PB3, SPI0_SCK
PB4	90	I/O	5VT	Default: NJTRST Alternate: SPI2_MISO, I2C0_TXFRAME Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	91	I/O	-	Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI
PB6	92	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, SPI0_IO2
PB7	93	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, TIMER3_CH1, EXMC_NL(NADV) Remap: USART0_RX, SPI0_IO3
BOOT0	94	I	-	Default: BOOT0
PB8	95	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, TIMER9_CH0 Remap: I2C0_SCL
PB9	96	I/O	5VT	Default: PB9 Alternate: TIMER3_CH3, TIMER10_CH0 Remap: I2C0_SDA
PE0	97	I/O	5VT	Default:PE0 Alternate: TIMER3_ETI, EXMC_NBL0
PE1	98	I/O	5VT	Default: PE1 Alternate: EXMC_NBL1

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{SS_3}	99	P	-	Default: V_{SS_3}
V_{DD_3}	100	P	-	Default: V_{DD_3}

Notes:

1. Type: I= input, O = output, P = power.
2. I/O Level: 5VT = 5V tolerant.
3. Functions are available in GD32E103xx devices.

2.6.2. GD32E103Rx LQFP64 pin definitions

Table 2-4. GD32E103Rx LQFP64 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{BAT}	1	P	-	Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O	-	Default: PC13 Alternate: RTC_TAMPER
PC14-OSC32IN	3	I/O	-	Default: PC14 Alternate:OSC32IN
PC15-OSC32OUT	4	I/O	-	Default: PC15 Alternate:OSC32OUT
PD0-OSCIN	5	I	-	Default: OSCIN Remap: PD0(3)
PD1-OSCOUT	6	O	-	Default: OSCOUT Remap: PD1(3)
NRST	7	I/O	-	Default: NRST
PC0	8	I/O	-	Default: PC0 Alternate: ADC01_IN10
PC1	9	I/O	-	Default: PC1 Alternate: ADC01_IN11
PC2	10	I/O	-	Default: PC2 Alternate: ADC01_IN12
PC3	11	I/O	-	Default: PC3 Alternate: ADC01_IN13
V_{SSA}	12	P	-	Default: V_{SSA}
V_{DDA}	13	P	-	Default: V_{DDA}
PA0-WKUP	14	I/O	-	Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI
PA1	15	I/O	-	Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1, TIMER1_CH1

Pin Name	Pins	Pin Type[(1)]	I/O Level[(2)]	Functions description
PA2	16	I/O	-	Default: PA2 Alternate: USART1_TX, TIMER4_CH2, ADC01_IN2, TIMER8_CH0, TIMER1_CH2, SPI0_IO2
PA3	17	I/O	-	Default: PA3 Alternate: USART1_RX, TIMER4_CH3, ADC01_IN3, TIMER1_CH3, TIMER8_CH1, SPI0_IO3
V_{SS_4}	18	P	-	Default: V_{SS_4}
V_{DD_4}	19	P	-	Default: V_{DD_4}
PA4	20	I/O	-	Default: PA4 Alternate: SPI0_NSS, USART1_CK, DAC_OUT0, ADC01_IN4 Remap: SPI2_NSS, I2S2_WS
PA5	21	I/O	-	Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1
PA6	22	I/O	-	Default: PA6 Alternate: SPI0_MISO, TIMER7_BRKIN, ADC01_IN6, TIMER2_CH0, TIMER12_CH0 Remap: TIMER0_BRKIN
PA7	23	I/O	-	Default: PA7 Alternate: SPI0_MOSI, TIMER7_CH0_ON, ADC01_IN7, TIMER2_CH1, TIMER13_CH0 Remap: TIMER0_CH0_ON
PC4	24	I/O	-	Default: PC4 Alternate: ADC01_IN14
PC5	25	I/O	-	Default: PC5 Alternate: ADC01_IN15
PB0	26	I/O	-	Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON Remap: TIMER0_CH1_ON
PB1	27	I/O	-	Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON Remap: TIMER0_CH2_ON
PB2	28	I/O	5VT	Default: PB2, BOOT1
PB10	29	I/O	5VT	Default: PB10 Alternate: I2C1_SCL, USART2_TX Remap: TIMER1_CH2
PB11	30	I/O	5VT	Default: PB11 Alternate: I2C1_SDA, USART2_RX Remap: TIMER1_CH3
V_{SS_1}	31	P	-	Default: V_{SS_1}
V_{DD_1}	32	P	-	Default: V_{DD_1}

Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
PB12	33	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2S1_WS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN
PB13	34	I/O	5VT	Default: PB13 Alternate: SPI1_SCK, I2S1_CK, USART2_CTS, TIMER0_CH0_ON, I2C1_TXFRAME
PB14	35	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0
PB15	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER0_CH2_ON, TIMER11_CH1
PC6	37	I/O	5VT	Default: PC6 Alternate: I2S1_MCK, TIMER7_CH0 Remap: TIMER2_CH0
PC7	38	I/O	5VT	Default: PC7 Alternate: I2S2_MCK, TIMER7_CH1 Remap: TIMER2_CH1
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER7_CH2 Remap: TIMER2_CH2
PC9	40	I/O	5VT	Default: PC9 Alternate: TIMER7_CH3 Remap: TIMER2_CH3
PA8	41	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, VCORE, USBFS_SOF, CTC_SYNC
PA9	42	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS
PA10	43	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, USBFS_ID, V1REF
PA11	44	I/O	5VT	Default: PA11 Alternate: USART0_CTS, USBFS_DM, TIMER0_CH3
PA12	45	I/O	5VT	Default: PA12 Alternate: USART0_RTS, USBFS_DP, TIMER0_ETI
PA13	46	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
V_{SS_2}	47	P	-	Default: V_{SS_2}
V_{DD_2}	48	P	-	Default: V_{DD_2}
PA14	49	I/O	5VT	Default: JTCK, SWCLK Remap:PA14

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA15	50	I/O	5VT	Default: JTDI Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, TIMER1_ETI, PA15, SPI0_NSS
PC10	51	I/O	5VT	Default: PC10 Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK
PC11	52	I/O	5VT	Default: PC11 Alternate: UART3_RX Remap: USART2_RX, SPI2_MISO
PC12	53	I/O	5VT	Default: PC12 Alternate: UART4_TX Remap: USART2_CK, SPI2_MOSI, I2S2_SD
PD2	54	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX
PB3	55	I/O	5VT	Default: JTDO Alternate: SPI2_SCK, I2S2_CK Remap: TIMER1_CH1, PB3, SPI0_SCK
PB4	56	I/O	5VT	Default: NJTRST Alternate: SPI2_MISO, I2C0_TXFRAME Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	57	I/O	-	Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI
PB6	58	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, SPI0_IO2
PB7	59	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, TIMER3_CH1 Remap: USART0_RX, SPI0_IO3
BOOT0	60	I	-	Default: BOOT0
PB8	61	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, TIMER9_CH0 Remap: I2C0_SCL
PB9	62	I/O	5VT	Default: PB9 Alternate: TIMER3_CH3, TIMER10_CH0 Remap: I2C0_SDA
V_{SS_3}	63	P	-	Default: V_{SS_3}
V_{DD_3}	64	P	-	Default: V_{DD_3}

Notes:

1. Type: I= input, O = output, P = power.

2. I/O Level: 5VT = 5V tolerant.
3. PD0/PD1 cannot be used for EXTI in this package.

2.6.3. GD32E103Cx LQFP48 pin definitions

Table 2-5. GD32E103Cx LQFP48 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{BAT}	1	P	-	Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O	-	Default: PC13 Alternate: RTC_TAMPER
PC14-OSC32IN	3	I/O	-	Default: PC14 Alternate:OSC32IN
PC15-OSC32OUT	4	I/O	-	Default: PC15 Alternate:OSC32OUT
PD0-OSCIN	5	I	-	Default: OSCIN Remap: PD0(3)
PD1-OSCOUT	6	O	-	Default: OSCOUT Remap: PD1(3)
NRST	7	I/O	-	Default: NRST
V_{SSA}	8	P	-	Default: V_{SSA}
V_{DDA}	9	P	-	Default: V_{DDA}
PA0-WKUP	10	I/O	-	Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0
PA1	11	I/O	-	Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1, TIMER1_CH1
PA2	12	I/O	-	Default: PA2 Alternate: USART1_TX, TIMER4_CH2, ADC01_IN2, TIMER8_CH0, TIMER1_CH2, SPI0_IO2
PA3	13	I/O	-	Default: PA3 Alternate: USART1_RX, TIMER4_CH3, ADC01_IN3, TIMER1_CH3, TIMER8_CH1, SPI0_IO3
PA4	14	I/O	-	Default: PA4 Alternate: SPI0_NSS, USART1_CK, DAC_OUT0, ADC01_IN4 Remap: SPI2_NSS, I2S2_WS
PA5	15	I/O	-	Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1
PA6	16	I/O	-	Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				TIMER12_CH0 Remap: TIMER0_BRKIN
PA7	17	I/O	-	Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1, TIMER13_CH0 Remap: TIMER0_CH0_ON
PB0	18	I/O	-	Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2 Remap: TIMER0_CH1_ON
PB1	19	I/O	-	Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3 Remap: TIMER0_CH2_ON
PB2	20	I/O	5VT	Default: PB2, BOOT1
PB10	21	I/O	5VT	Default: PB10 Alternate: I2C1_SCL, USART2_TX Remap: TIMER1_CH2
PB11	22	I/O	5VT	Default: PB11 Alternate: I2C1_SDA, USART2_RX Remap: TIMER1_CH3
V_{SS_1}	23	P	-	Default: V_{SS_1}
V_{DD_1}	24	P	-	Default: V_{DD_1}
PB12	25	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2S1_WS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN
PB13	26	I/O	5VT	Default: PB13 Alternate: SPI1_SCK, I2S1_CK, USART2_CTS, TIMER0_CH0_ON, I2C1_TXFRAME
PB14	27	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0
PB15	28	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER0_CH2_ON, TIMER11_CH1
PA8	29	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, VCORE, USBFS_SOF, CTC_SYNC
PA9	30	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS
PA10	31	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, USBFS_ID, V1REF

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA11	32	I/O	5VT	Default: PA11 Alternate: USART0_CTS, USBFS_DM, TIMER0_CH3
PA12	33	I/O	5VT	Default: PA12 Alternate: USART0_RTS, USBFS_DP, TIMER0_ETI
PA13	34	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
V_{SS_2}	35	P	-	Default: V_{SS_2}
V_{DD_2}	36	P	-	Default: V_{DD_2}
PA14	37	I/O	5VT	Default: JTCK, SWCLK Remap:PA14
PA15	38	I/O	5VT	Default: JTDI Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, TIMER1_ETI, PA15, SPI0_NSS
PB3	39	I/O	5VT	Default: JTDO Alternate: SPI2_SCK, I2S2_CK Remap: TIMER1_CH1, PB3, SPI0_SCK
PB4	40	I/O	5VT	Default: NJTRST Alternate: SPI2_MISO, I2C0_TXFRAME Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	41	I/O	-	Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI
PB6	42	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, SPI0_IO2
PB7	43	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, TIMER3_CH1 Remap: USART0_RX, SPI0_IO3
BOOT0	44	I	-	Default: BOOT0
PB8	45	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, TIMER9_CH0 Remap: I2C0_SCL
PB9	46	I/O	5VT	Default: PB9 Alternate: TIMER3_CH3, TIMER10_CH0 Remap: I2C0_SDA
V_{SS_3}	47	P	-	Default: V_{SS_3}
V_{DD_3}	48	P	-	Default: V_{DD_3}

Notes:

1. Type: I= input, O = output, P = power.
2. I/O Level: 5VT = 5V tolerant.

3. PD0/PD1 cannot be used for EXTI in this package.

2.6.4. GD32E103Tx QFN36 pin definitions

Table 2-6. GD32E103Tx LQFP36 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PD0-OSCIN	2	I	-	Default: OSCIN Remap: PD0(3)
PD1-OSCOUT	3	O	-	Default: OSCOUT Remap: PD1(3)
NRST	4	I/O	-	Default: NRST
V_{SSA}	5	P	-	Default: V_{SSA}
V_{DDA}	6	P	-	Default: V_{DDA}
PA0-WKUP	7	I/O	-	Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0
PA1	8	I/O	-	Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1, TIMER1_CH1
PA2	9	I/O	-	Default: PA2 Alternate: USART1_TX, TIMER4_CH2, ADC01_IN2, TIMER1_CH2, SPI0_IO2
PA3	10	I/O	-	Default: PA3 Alternate: USART1_RX, TIMER4_CH3, ADC01_IN3, TIMER1_CH3, SPI0_IO3
PA4	11	I/O	-	Default: PA4 Alternate: SPI0_NSS, USART1_CK, DAC_OUT0, ADC01_IN4
PA5	12	I/O	-	Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1
PA6	13	I/O	-	Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0 Remap: TIMER0_BRKIN
PA7	14	I/O	-	Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1 Remap: TIMER0_CH0_ON
PB0	15	I/O	-	Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2 Remap: TIMER0_CH1_ON
PB1	16	I/O	-	Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3 Remap: TIMER0_CH2_ON

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB2	17	I/O	5VT	Default: PB2, BOOT1
V_{SS_1}	18	P	-	Default: V_{SS_1}
V_{DD_1}	19	P	-	Default: V_{DD_1}
PA8	20	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, VCORE, USBFS_SOF, CTC_SYNC
PA9	21	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS
PA10	22	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, USBFS_ID, V1REF
PA11	23	I/O	5VT	Default: PA11 Alternate: USART0_CTS, USBFS_DM, TIMER0_CH3
PA12	24	I/O	5VT	Default: PA12 Alternate: USART0_RTS, USBFS_DP, TIMER0_ETI
PA13	25	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
V_{SS_2}	26	P	-	Default: V_{SS_2}
V_{DD_2}	27	P	-	Default: V_{DD_2}
PA14	28	I/O	5VT	Default: JTCK, SWCLK Remap:PA14
PA15	29	I/O	5VT	Default: JTDI Remap: TIMER1_CH0, TIMER1_ETI, TIMER1_ETI, PA15, SPI0_NSS
PB3	30	I/O	5VT	Default: JTDO Remap: TIMER1_CH1, PB3, SPI0_SCK
PB4	31	I/O	5VT	Default: NJTRST Alternate: I2C0_TXFRAME Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	32	I/O	-	Default: PB5 Alternate: I2C0_SMBA Remap: TIMER2_CH1, SPI0_MOSI
PB6	33	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, SPI0_IO2
PB7	34	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, TIMER3_CH1 Remap: USART0_RX, SPI0_IO3

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
BOOT0	35	I	-	Default: BOOT0
V_{SS_3}	36	P	-	Default: V_{SS_3}
V_{DD_3}	1	P	-	Default: V_{DD_3}

Notes:

1. Type: I= input, O = output, P = power.
2. I/O Level: 5VT = 5V tolerant.
3. PD0/PD1 cannot be used for EXTI in this package.

3. Functional description

3.1. Arm® Cortex®-M4 core

The Arm® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring floating point operations, memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit Arm® Cortex®-M4 processor core

- Up to 120 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Floating Point Unit (FPU)
- Integrated DSP instructions
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M4 processor is based on the ARMv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2. On-chip memory

- Up to 128 Kbytes of Flash memory
- Up to 32 KB of SRAM

The Arm® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 128 Kbytes of inner Flash at most, which includes code Flash that available for storing programs and data, and accessed (R/W) at CPU clock speed. An extra data Flash is also included for storing data mainly. ***Table 2-2. GD32E103xx memory map*** shows the memory of the GD32E103xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- 1.71 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 120MHz. The maximum frequency of the two APB domains including APB1 is 60 MHz and APB2 is 120 MHz. See ***Figure 2-6. GD32E103xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.66V/down to 1.62V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.71 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} range: 1.71 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.71 to 3.6 V, power supply for RTC, external clock 32.768 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10).

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep mode, Deep-sleep mode, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode

  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

- **Deep-sleep** mode

  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, IRC48M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.

- **Standby** mode

  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, IRC48M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup Registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDG reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 3 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: V_{REF-} to V_{REF+}
- Temperature sensor

Up to two 12-bit 3 MSPS multi-channel ADCs are integrated in the device. It has a total of 18 multiplexed channels: 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}, V_{REFINT} = 1.2V). The input voltage range is from V_{REF-} to V_{REF+}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx, x=1, 2, 3) and the advanced timers (TIMER0 and TIMER7) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7. Digital to analog converter (DAC)

- 12-bit DAC with independent output channels
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC is used to generate variable analog outputs. The DAC channels can be triggered by the timer or EXTI with DMA support. In dual DAC channel operation, conversions could be done independently or simultaneously. The maximum output value of the DAC is V_{REF+}.

3.8. DMA

- 7 channel DMA0 controller and 5 channel DMA1 controller
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs, DAC, I2S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9. General-purpose inputs/outputs (GPIOs)

- Up to 80 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 80 general purpose I/O pins (GPIO) in GD32E103xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15 and PE0 ~ PE15 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10. Timers and PWM generation

- Two 16-bit advanced timer (TIMER0 & TIMER7), ten 16-bit general timers (TIMER1 ~ TIMER4, TIMER8 ~ TIMER13), and two 16-bit basic timer (TIMER5 & TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer, can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 ~ TIMER4 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER8 ~ TIMER13 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 &TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32E103xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11. Real time clock (RTC)

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wake-up event

The real time clock is an independent timer which provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.12. Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides several data transfer rates: up to 100 KHz of standard mode, up to 400 KHz of the fast mode and up to 1 MHz of the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13. Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad-SPI configuration available in master mode (only in SPI0)
- SPI TI mode and NSS pulse mode supported

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14. Universal synchronous asynchronous receiver transmitter (USART)

- Up to three USARTs and two UARTs with operating frequency up to 7.5MBits/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- USARTs support ISO 7816-3 compliant smart card interface

The USART (USART0, USART1 and USART2) and UART (UART3 & UART4) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication except UART4.

3.15. Inter-IC sound (I2S)

- Two I2S bus interfaces with sampling frequency from 8 KHz to 192 KHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32E103xx contain two I2S-bus interfaces that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequency from 8 KHz to 192 KHz is supported.

3.16. Universal serial bus full-speed interface (USBFS)

- One full-speed USB Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator support crystal-less operation
- Internal main PLL for USB CLK compliantly

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports device modes. The status of a completed USB transfer or error condition is indicated by status registers. An interrupt is also generated if enabled. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode that allows crystal-less operation.

3.17. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash
- Up to 16-bit data bus
- Support to interface with Motorola 6800 and Intel 8080 type LCD directly

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC support code execution from external memory. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.18. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.19. Package and operation temperature

- LQFP100 (GD32E103Vx), LQFP64 (GD32E103Rx) and LQFP48 (GD32E103Cx) QFN36 (GD32E103Tx)
- Operation temperature range: -40°C to +85°C (industrial level)

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings(1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS} - 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	3.6	V
$\lvert\Delta V_{DDX}\rvert$	Variations between different V_{DD} power pins	—	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	±25	mA
T_A	Operating temperature range	-40	+85	°C
P_D	Power dissipation at T_A = 85°C of LQFP100	—	813	mW
	Power dissipation at T_A = 85°C of LQFP64	—	733	
	Power dissipation at T_A = 85°C of LQFP48	—	574	
	Power dissipation at T_A = 85°C of QFN36	—	1086	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Guaranteed by design, not tested in production.
(2) All main power and ground pins should be connected to an external power source within the allowable range.
(3) V_{IN} maximum value cannot exceed 5.5 V.
(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

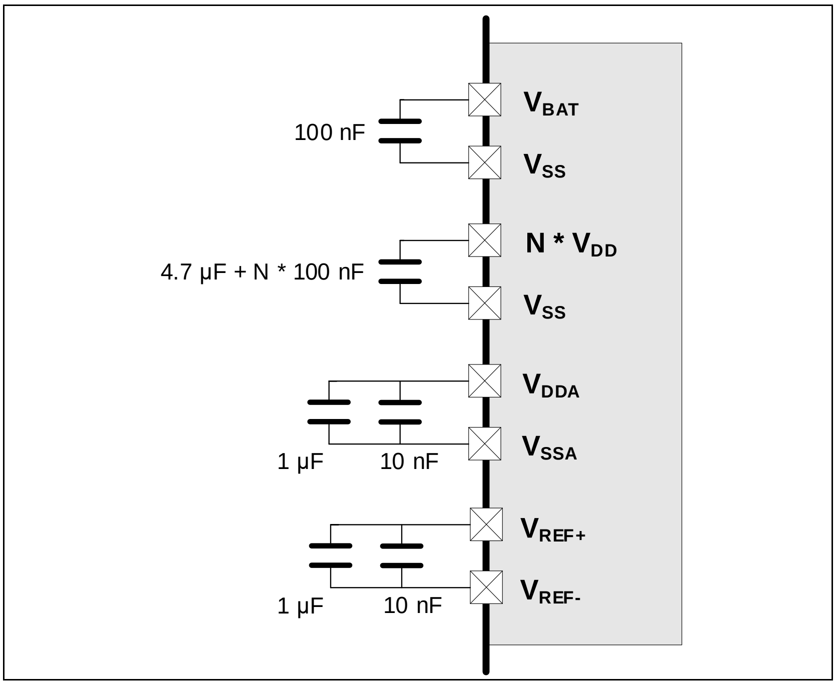
4.2. Operating conditions characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	—	1.71	3.3	3.6	V
V_{DDA}	Analog supply voltage ADC not used	—	1.71	3.3	3.6	V
	Analog supply voltage ADC used		2.4	3.3	3.6	
V_{BAT}	Battery supply voltage	—	1.71	—	3.6	V

(1) Guaranteed by design, not tested in production.

Figure 4-1. Recommended power supply decoupling capacitors(1)(2)



(1) The V_{REF+} and V_{REF-} pins are only available on no less than 100-pin packages, or else the V_{REF+} and V_{REF-} pins are not available and internally connected to V_{DDA} and V_{SSA} pins.
(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	—	—	120	MHz
f_{APB1}	APB1 clock frequency	—	—	60	MHz
f_{APB2}	APB2 clock frequency	—	—	120	MHz

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up/ Power down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	μs/V
	V_{DD} fall time rate		20	∞	

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions(1)(2)(3)

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	468	μs
		Clock source from IRC8M	86.8	

(1) Based on characterization, not tested in production.
(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.
(3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics(1)(2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	4.3	μs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode（LDO On）	18.0	

Symbol	Parameter	Typ	Unit
	Wakeup from Deep-sleep mode（LDO in low power mode）	18.0	
$t_{Standby}$	Wakeup from Standby mode	82.0	

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC8M = System clock = 8 MHz.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics(2)(3)(4)(5)

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
$I_{DD}+I_{DDA}$	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock=120 MHz, All peripherals enabled	—	28.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals disabled	—	16.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals enabled	—	24.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals disabled	—	14.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals enabled	—	22.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals disabled	—	13.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals enabled	—	17.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals disabled	—	10.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals enabled	—	12.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals disabled	—	8.1	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals enabled	—	9.8	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals disabled	—	6.7	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 24 MHz, All peripherals enabled	—	7.4	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 24 MHz, All peripherals disabled	—	5.3	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals enabled	—	5.7	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals disabled	—	4.4	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals enabled	—	4.1	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals disabled	—	3.4	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals enabled	—	1.3	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals disabled	—	1.0	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 2 MHz, System clock = 2 MHz, All peripherals enabled	—	0.9	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 2 MHz, System Clock = 2 MHz, All peripherals disabled	—	0.7	—	mA
	Supply current (Sleep mode)	$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals enabled	—	20.5	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals disabled	—	6.9	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals enabled	—	18.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals disabled	—	6.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals enabled	—	16.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals disabled	—	5.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 72 MHz, CPU clock off, All peripherals enabled	—	13	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 72 MHz, CPU clock off, All peripherals disabled	—	5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals enabled	—	9.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals disabled	—	4.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals enabled	—	7.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals disabled	—	3.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 24 MHz, CPU clock off, All peripherals enabled	—	5.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 24 MHz, CPU clock off, All peripherals disabled	—	3.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 16 MHz, CPU clock off, All peripherals enabled	—	4.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 16 MHz, CPU clock off, All peripherals disabled	—	3	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 8 MHz, CPU clock off, All peripherals enabled	—	3.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 8 MHz, CPU clock off, All peripherals disabled	—	2.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System Clock = 4 MHz, CPU clock off, All peripherals enabled	—	1.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System Clock = 4 MHz, CPU clock off, All peripherals disabled	—	0.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System Clock = 2 MHz, CPU clock off, All peripherals enabled	—	0.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System Clock = 2 MHz, CPU clock off, All peripherals disabled	—	0.6	—	mA
	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in normal power mode, IRC40K off, RTC off, All GPIOs analog mode	—	41.8	550	μA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power mode, IRC40K off, RTC off, All GPIOs analog mode	—	31.8	550	μA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC on	—	2.1	11	μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC off	—	2.0	11	μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K off, RTC off	—	1.5	11	μA
I_{BAT}	Battery supply current (Backup mode)	V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.6	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.4	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.3	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.71 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.2	—	μA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.3	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.1	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.0	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.71 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	0.9	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	1.0	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	0.9	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	0.7	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.71 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	0.6	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	0.9	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	0.8	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	0.6	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.71 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	0.5	—	μA

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for T_A = 25 ℃ and test result is mean value.

(3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(4) When System Clock is greater than 8 MHz, a crystal 25 MHz is used, and the HXTAL bypass function is closed, using PLL.

(5) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additionalpower consumption should be considered.

Figure 4-2. Typical supply current consumption in Run mode

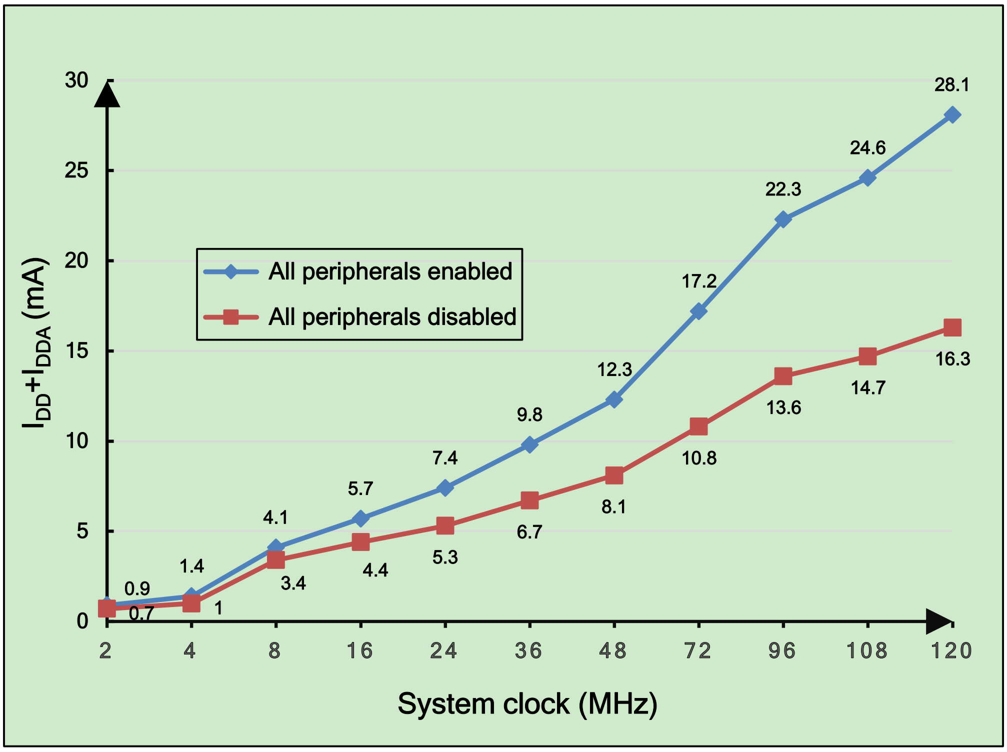


Figure 4-3. Typical supply current consumption in Sleep mode

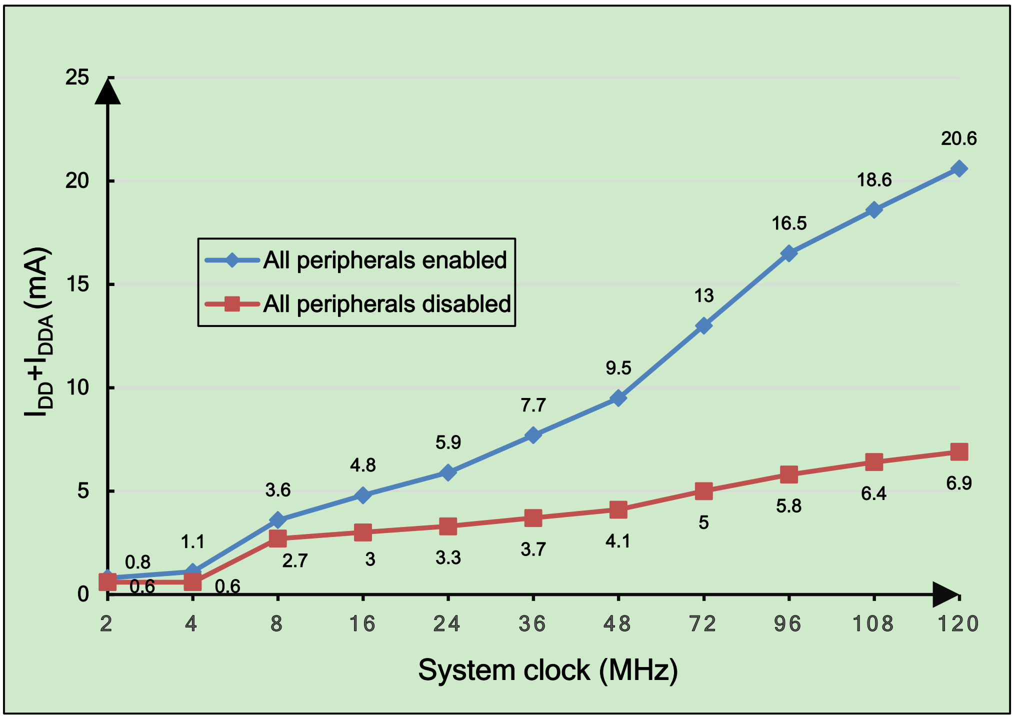


Table 4-8. Peripheral current consumption characteristics(1)

Peripherals(4)		Typical consumption at 25 ℃（TYP）	Unit
APB1	DAC(2)	0.44	mA

Peripherials[(4)]		Typical consumption at 25 ℃（TYP）	Unit
	PMU	0.18	
	BKPI	0.38	
	I2C1	0.77	
	I2C0	0.77	
	UART4	0.78	
	UART3	0.78	
	USART2	0.78	
	USART1	0.78	
	SPI2	0.72	
	SPI1	0.78	
	WWDGT	0.03	
	TIMER13	0.32	
	TIMER12	0.3	
	TIMER11	0.31	
	TIMER6	0.05	
	TIMER5	0.04	
	TIMER4	0.38	
	TIMER3	0.37	
	TIMER2	0.36	
	TIMER1	0.37	
ADDAPB1	CTC	0.68	
APB2	TIMER10	0.56	
	TIMER9	0.58	
	TIMER8	0.6	
	USART0	0.52	
	TIMER7	0.87	
	SPI0	0.09	
	TIMER0	0.65	
	ADC1[(3)]	1.36	
	ADC0[(3)]	1.35	
	GPIOE	0.18	
	GPIOD	0.19	
	GPIOC	0.2	
	GPIOB	0.18	
	GPIOA	0.19	
	GPIOF	0.04	
AHB	USBFS	1.48	
	EXMC	0.29	
	CRC	0.03	
	DMA1	0.31	
	DMA0	0.39	

(1) Based on characterization, not tested in production.
(2) DEN0 and DEN1 bits in the DAC_CTL register are set to 1, and the converted value set to 0x800.
(3) System clock = f_{HCLK} = 72 MHz, f_{APB1} = $f_{HCLK}/2$, f_{APB2} = f_{HCLK}, f_{ADCCLK} = $f_{APB2}/2$, ADCON bit is set to 1.
(4) If there is no other description, then HXTAL = 25 MHz, system clock = f_{HCLK} = 120 MHz, f_{APB1} = $f_{HCLK}/2$, f_{APB2} = f_{HCLK}.

4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the *Table 4-9. EMS characteristics*(1), based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-9. EMS characteristics(1)

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100, f_{HCLK} = 120 MHz conforms to IEC 61000-4-2	3A
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	V_{DD}= 3.3 V, T_A = 25 °C, LQFP100, f_{HCLK} = 120 MHz conforms to IEC 61000-4-4	4A

(1) Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-10. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low voltage Detector Threshold	LVDT<2:0> = 000(rising edge)	—	2.07	—	V
		LVDT<2:0> = 000(falling edge)	—	1.97	—	
		LVDT<2:0> = 001(rising edge)	—	2.2	—	
		LVDT<2:0> = 001(falling edge)	—	2.1	—	
		LVDT<2:0> = 010(rising edge)	—	2.34	—	
		LVDT<2:0> = 010(falling edge)	—	2.24	—	
		LVDT<2:0> = 011(rising edge)	—	2.47	—	
		LVDT<2:0> = 011(falling edge)	—	2.37	—	
		LVDT<2:0> = 100(rising edge)	—	2.61	—	
		LVDT<2:0> = 100(falling edge)	—	2.51	—	
		LVDT<2:0> = 101(rising edge)	—	2.74	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		LVDT<2:0> = 101(falling edge)	—	2.64	—	
		LVDT<2:0> = 110(rising edge)	—	2.88	—	
		LVDT<2:0> = 110(falling edge)	—	2.78	—	
		LVDT<2:0> = 111(rising edge)	—	3.01	—	
		LVDT<2:0> = 111(falling edge)	—	2.91	—	
$V_{LVDhyst}$(2)	LVD hystersis	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	1.67	—	V
V_{PDR}(1)	Power down reset threshold		—	1.62	—	V
$V_{PDRhyst}$(2)	PDR hysteresis		—	40	—	mV
$t_{RSTTEMPO}$(2)	Reset temporization		—	2	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-11. ESD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; JS-001-2014	—	—	5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; JS-002-2014	—	—	800	V

(1) Based on characterization, not tested in production.

Table 4-12. Static latch-up characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A = 25 °C; JESD78	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

(1) Based on characterization, not tested in production.

4.7. External clock characteristics

Table 4-13. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL} (1)	Crystal or ceramic frequency	1.71 ≤ V_{DD} ≤ 3.6 V	4	8	32	MHz
R_F (2)	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL} (2) (3)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$ (2)	Crystal or ceramic duty cycle	—	30	50	70	%
g_m (2)	Oscillator transconductance	Startup	—	25	—	mA/V
$I_{DD(HXTAL)}$ (1)	Crystal or ceramic operating current	V_{DD} = 3.3 V	—	1.1	—	mA
$t_{SUHXTAL}$ (1)	Crystal or ceramic startup time	V_{DD} = 3.3 V	—	1.8	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

Table 4-14. High speed external clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext} (1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	1	—	50	MHz
V_{HXTALH} (2)	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL} (2)	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	V
$t_{H/L(HXTAL)}$ (2)	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$ (2)	OSCIN rise or fall time	—	—	—	10	ns
C_{IN} (2)	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$ (2)	Duty cycle	—	40	—	60	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}(1)	Crystal or ceramic frequency	V_{DD} = 3.3 V	—	32.768	—	kHz
C_{LXTAL}(2) (3)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	10	—	pF
$Ducy_{(LXTAL)}$ (2)	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(2)	Oscillator transconductance	Lower driving capability	—	4	—	µA/V
		Medium low driving capability	—	6	—	
		Medium high driving capability	—	12	—	
		Higher driving capability	—	18	—	
$I_{DDLXTAL}$ (1)	Crystal or ceramic operating current	Lower driving capability	—	0.7	—	µA
		Medium low driving capability	—	0.8	—	
		Medium high driving capability	—	1.1	—	
		Higher driving capability	—	1.4	—	
$t_{SULXTAL}$(1) (4)	Crystal or ceramic startup time	—	—	1.8	—	s

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.
(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-16.Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}(2)	OSC32IN input pin high level voltage	—	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}(2)	OSC32IN input pin low level voltage	—	V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$ (2)	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$ (2)	OSC32IN rise or fall time	—	—	—	50	
C_{IN}(2)	OSC32IN input capacitance	—	—	5	—	pF
$Ducy_{(LXTAL)}$ (2)	Duty cycle	—	30	50	70	%

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.8. Internal clock characteristics

Table 4-17. High speed internal clock (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C(1)	-2.5	—	+2.5	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 0 °C ~ +85 °C(1)	-1.8	—	+1.8	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.0	—	+1.0	%
	IRC8M oscillator Frequency accuracy, User trimming step(1)	—	—	0.3	—	%
$Ducy_{IRC8M}$(2)	IRC8M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC8M}$(1)	IRC8M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{IRC8M} = 8 MHz	—	110	—	μA
$t_{SUIRC8M}$(1)	IRC8M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{IRC8M} = 8 MHz	—	2	—	μs

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Table 4-18. Low speed internal clock (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}(1)	Low Speed Internal oscillator (IRC40K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C	28	40	60	kHz
$I_{DDAIRC40K}$(2)	IRC40K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	0.42	—	μA
$t_{SUIRC40K}$(2)	IRC40K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	110	—	μs

(1) Guaranteed by design, not tested in production.
(2) Based on characterization, not tested in production.

Table 4-19. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	$V_{DD} = V_{DDA} = 3.3$ V	—	48	—	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	$V_{DD} = V_{DDA} = 3.3$ V, $T_A = -40$ °C ~ +85 °C(1)	-4.0	—	5.0	%
		$V_{DD} = V_{DDA} = 3.3$ V, $T_A = 0$ °C ~ +85 °C(1)	-3.0	—	3.0	%
		$V_{DD} = V_{DDA} = 3.3$ V, $T_A = 25$ °C	-2.0	—	2.0	%
	IRC48M oscillator Frequency accuracy, User trimming step(1)	—	—	0.1	—	%
$Ducy_{IRC48M}$(2)	IRC48M oscillator duty cycle	$V_{DD} = V_{DDA} = 3.3$ V	45	50	55	%
$I_{DDIRC48M}$(1)	IRC48M oscillator operating current	$V_{DD} = V_{DDA} = 3.3$ V, $f_{IRC48M} = 48$ MHz	—	270	—	μA
$t_{SUIRC48M}$(1)	IRC48M oscillator startup time	$V_{DD} = V_{DDA} = 3.3$ V, $f_{IRC48M} = 48$ MHz	—	2.5	—	μs

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.9. PLL characteristics

Table 4-20. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	1	8	25	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	16	—	120	MHz
f_{VCO}(2)	VCO output frequency	—	32	—	240	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	μs
I_{DDA}(1)	Current consumption on V_{DDA}	VCO freq = 240 MHz	—	350	—	μA
$Jitter_{PLL}$(1)(3)	Cycle to cycle Jitter （rms）	System clock	—	46	—	ps
	Cycle to cycle Jitter （peak to peak）		—	463	—	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Value given with main PLL running.

Table 4-21. PLL1/2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	1	8	25	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	16	—	120	MHz
f_{VCO}(2)	VCO output frequency	—	32	—	240	MHz

t_{LOCK}(2)	PLL lock time	—	—	—	300	μs
I_{DDA}(1)	Current consumption on V_{DDA}	VCO freq = 240 MHz	—	320	—	μA
$Jitter_{PLL}$(1)(3)	Cycle to cycle Jitter （rms）	System clock	—	46	—	ps
	Cycle to cycle Jitter （peak to peak）		—	463	—	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Value given with main PLL running.

4.10. Memory characteristics

Table 4-22. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}(1)	Number of guaranteed program /erase cycles before failure(Endurance)	T_A = -40 °C ~ +85 °C	100	—	—	kcycles
t_{RET}(1)	Data retention time	10k cycles at T_A = 85 °C	10	—	—	years
t_{PROG}(2)	Word(3) programming time	T_A = -40 °C ~ +85 °C	37	—	44	μs
t_{ERASE}(2)	Page erase time	T_A = -40 °C ~ +85 °C	3.2	—	4	ms
t_{MERASE}(2)	Mass erase time	T_A = -40 °C ~ +85 °C	8	—	10	ms

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Word is 32 bits or 64 bits depend on PGW bit in FMC_WS register.

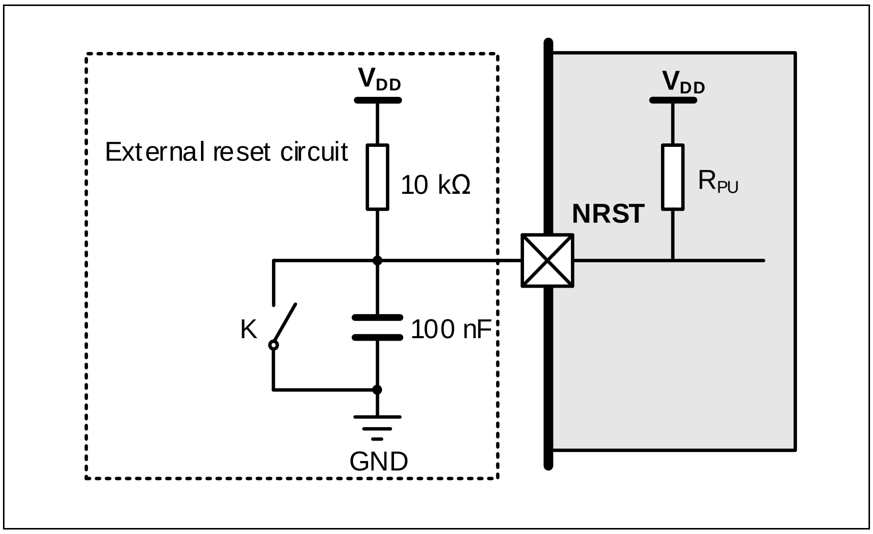
4.11. NRST pin characteristics

Table 4-23. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	-0.5	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.45	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	460	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit



4.12. GPIO characteristics

Table 4-24. I/O port DC characteristics(1)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
	5V-tolerant IO Low level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
V_{IH}	Standard IO High level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
	5V-tolerant IO High level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
V_{OL}	Low level output voltage (I_{IO} = +8 mA)	V_{DD} = 1.8 V	—	—	0.32	V
		V_{DD} = 2.5 V	—	—	0.24	
		V_{DD} = 3.3 V	—	—	0.11	
		V_{DD} = 3.6 V	—	—	0.11	
V_{OL}	Low level output voltage (I_{IO} = +20 mA)	V_{DD} = 1.8 V	—	—	0.53	V
		V_{DD} = 2.5 V	—	—	0.60	
		V_{DD} = 3.3 V	—	—	0.28	
		V_{DD} = 3.6 V	—	—	0.27	
V_{OH}	High level output voltage (I_{IO} = +8 mA)	V_{DD} = 1.8 V	1.49	—	—	V
		V_{DD} = 2.5 V	2.27	—	—	
		V_{DD} = 3.3 V	3.14	—	—	
		V_{DD} = 3.6 V	3.45	—	—	
V_{OH}	High level output voltage (I_{IO} = +20 mA)	V_{DD} = 1.8 V	1.25	—	—	V
		V_{DD} = 2.5 V	1.89	—	—	
		V_{DD} = 3.3 V	2.91	—	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		V_{DD} = 3.6 V	3.23	—	—	
R_{PU}(2)	Internal pull-up resistor	—	—	40	—	kΩ
R_{PD}(2)	Internal pull-down resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

Table 4-25. I/O port AC characteristics(1)(2)

GPIOx_MDy[1:0] bit value(3)	Parameter	Conditions	Max	Unit
GPIOx_CTL->MDy[1:0] = 10 （IO_Speed = 2 MHz）	Maximum frequency(4)	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	9	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	6	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	4	
GPIOx_CTL->MDy[1:0] = 01 （IO_Speed = 10 MHz）	Maximum frequency(4)	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	50	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	25	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	15	
GPIOx_CTL->MDy[1:0] = 11 （IO_Speed = 50 MHz）	Maximum frequency(4)	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	60	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	30	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	20	
GPIOx_CTL->MDy[1:0] = 11 and GPIOx_SPDy = 1 （IO_Speed = MAX）	Maximum frequency(4)	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	70	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	50	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	30	

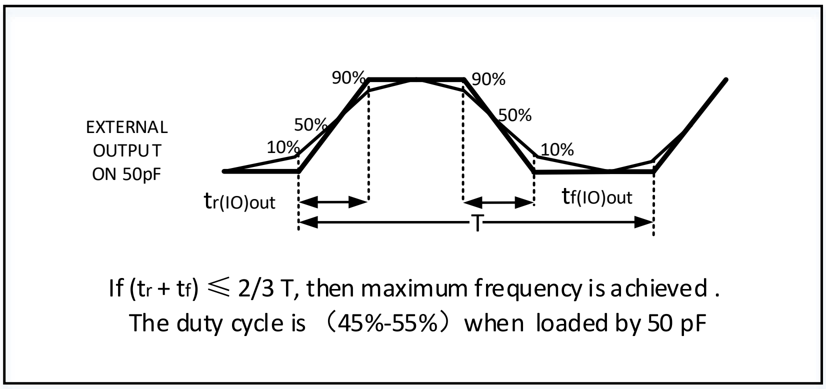
(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all test results given for T_A = 25 ℃.

(3) The I/O speed is configured using the GPIOx_CTL -> MDy[1:0] bits. Refer to the GD32E103xx user manual which is selected to set the GPIO port output speed.

(4) The maximum frequency is defined in *Figure 4-5. I/O port AC characteristics definition*

Figure 4-5. I/O port AC characteristics definition



4.13. ADC characteristics

Table 4-26. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	2.4	3.3	3.6	V
V_{IN}(1)	ADC input voltage range	—	0	—	V_{REF+}	V
f_{ADC}(1)	ADC clock	—	0.1	—	42	MHz
f_S(1)	Sampling rate	12-bit	0.007	—	3	MSPS
		10-bit	0.008	—	3.5	
		8-bit	0.01	—	4.2	
		6-bit	0.011	—	5.25	
V_{AIN}(1)	Analog input voltage	16 external; 2 internal	0	—	V_{DDA}	V
V_{REF+}(2)	Positive Reference Voltage	—	1.8	—	V_{DDA}	V
V_{REF-}(2)	Negative Reference Voltage	—	—	V_{SSA}	—	V
R_{AIN}(2)	External input impedance	See ***Equation 1***	—	—	24	kΩ
R_{ADC}(2)	Input sampling switch resistance	—	—	—	0.2	kΩ
C_{ADC}(2)	Input sampling capacitance	No pin/pad capacitance included	—	—	5.5	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 42 MHz	—	3.12	—	μs
t_s(2)	Sampling time	f_{ADC} = 42 MHz	0.036	—	5.7	μs
t_{CONV}(2)	Total conversion time(including sampling time)	12-bit	—	14	—	1/ f_{ADC}
		10-bit	—	12	—	
		8-bit	—	10	—	
		6-bit	—	8	—	
t_{SU}(2)	Startup time	—	—	—	1	μs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-27. ADC R_{AIN} max for f_{ADC} = 42 MHz

T_s(cycles)	t_s(us)	R_{AINmax} (kΩ)
1.5	0.04	0.47
7.5	0.18	3.15
13.5	0.32	5.82
28.5	0.68	12.55
41.5	0.99	18.35
55.5	1.32	24.55
71.5	1.70	NA

T_s(cycles)	t_s(us)	R_{AINmax} (kΩ)
239.5	5.70	NA

Table 4-28. ADC dynamic accuracy at f_{ADC} = 14 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 14 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 20 kHz Temperature = 25 ℃	—	10.3	—	bits
SNDR	Signal-to-noise and distortion ratio		—	63.8	—	dB
SNR	Signal-to-noise ratio		—	64.5	—	
THD	Total harmonic distortion		—	-67.5	—	

(1) Based on characterization, not tested in production.

Table 4-29. ADC dynamic accuracy at f_{ADC} = 42 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 42 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 20 kHz Temperature = 25 ℃	—	10.3	—	bits
SNDR	Signal-to-noise and distortion ratio		—	63.8	—	dB
SNR	Signal-to-noise ratio		—	64.5	—	
THD	Total harmonic distortion		—	-67.5	—	

(1) Based on characterization, not tested in production.

Table 4-30. ADC static accuracy at f_{ADC} = 42 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 42 MHz V_{DDA} = V_{REF+} = 3.3 V	±1	—	LSB
DNL	Differential linearity error		±1	—	
INL	Integral linearity error		±3	—	

(1) Based on characterization, not tested in production.

4.14. Temperature sensor characteristics

Table 4-31. Temperature sensor characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±1.5	—	℃
Avg_Slope	Average slope	—	4.3	—	mV/℃
V_{25}	Voltage at 25 °C	—	1.47	—	V
t_{START}	Startup time	—	—	—	μs
t_{S_temp}(2)	ADC sampling time when reading the temperature	—	17.1	—	μs

(1) Based on characterization, not tested in production.
(2) Shortest sampling time can be determined in the application by multiple iterations.

4.15. DAC characteristics

Table 4-32. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	1.71	3.3	3.6	V
V_{REF+}(1)	Reference supply voltage	—	1.8	—	V_{DDA}	V
V_{REF-}(1)	Negative Reference Voltage	—	—	V_{SSA}	—	V
R_{LOAD}(2)	Load resistance	Resistive load with buffer ON	5	—	—	kΩ
R_O(2)	Impedance output with buffer OFF	—	—	—	15	kΩ
C_{LOAD}(2)	Load capacitance	No pin/pad capacitance included	—	—	50	pF
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	—	0.2	—	—	V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	—	—	—	V_{DDA}-0.2	V
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	—	—	0.5	—	mV
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	—	—	—	V_{DDA}-1LSB	V
I_{DDA}(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 3.6 V	—	380	—	μA
		With no load, worst code(0xF1C) on the input, V_{REF+} = 3.6 V	—	460	—	μA
$I_{DDVREF+}$(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 3.6 V	—	120	—	μA
		With no load, worst code(0xF1C) on the input, V_{REF+} = 3.6 V	—	320	—	μA
DNL(1)	Differential non-linearity error	DAC in 12-bit mode	—	—	±3	LSB
INL(1)	Integral non-linearity	DAC in 12-bit mode	—	—	±4	LSB
Offset(1)	Offset error	DAC in 12-bit mode	—	—	±12	LSB
GE(1)	Gain error	DAC in 12-bit mode	—	—	±0.5	%
$T_{setting}$(1)	Settling time	C_{LOAD} ⩽ 50 pF, R_{LOAD} ⩾ 5 kΩ	—	0.3	1	μs
T_{wakeup}(2)	Wakeup from off state	—	—	5	10	μs
Update rate(2)	Max frequency for a correct DAC_OUT change from code i to i±1LSBs	C_{LOAD} ⩽ 50 pF, R_{LOAD} ⩾ 5 kΩ	—	—	4	MS/s
PSRR(2)	Power supply rejection ratio	—	55	80	—	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	(to V_{DDA})					

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.16. I2C characteristics

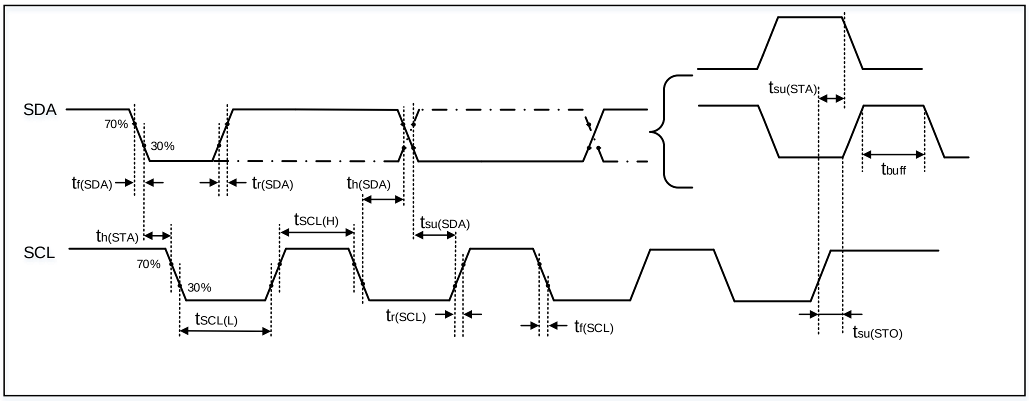
Table 4-33. I2C characteristics(1)(2)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{su(SDA)}$	SDA setup time	—	2	—	0.8	—	0.1	—	μs
$t_{h(SDA)}$	SDA data hold time	—	250	—	250	—	130	—	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	20	300	—	120	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs

(1) Guaranteed by design, not tested in production

(2) Test condition: GPIO_SPEED set 2 MHz and external pull-up resistor value is 1 kΩ when operate EEPROM with I2C.

Figure 4-6. I2C bus timing diagram



4.17. SPI characteristics

Table 4-34. Standard SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	30	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 120 MHz, presc = 8	31.83	33.33	34.83	ns

$t_{SCK(L)}$	SCK clock low time	Master mode, f_{PCLKx} = 120 MHz, presc = 8	31.83	33.33	34.83	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	7	—	ns
$t_{H(MO)}$	Data output hold time	—	—	4	—	ns
$t_{SU(MI)}$	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	9	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	8	—	ns
$t_{V(SO)}$	Data output valid time	—	—	10	—	ns
$t_{H(SO)}$	Data output hold time	—	—	10	—	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	2	—	—	ns

(1) Based on characterization, not tested in production.

Figure 4-7. SPI timing diagram - master mode

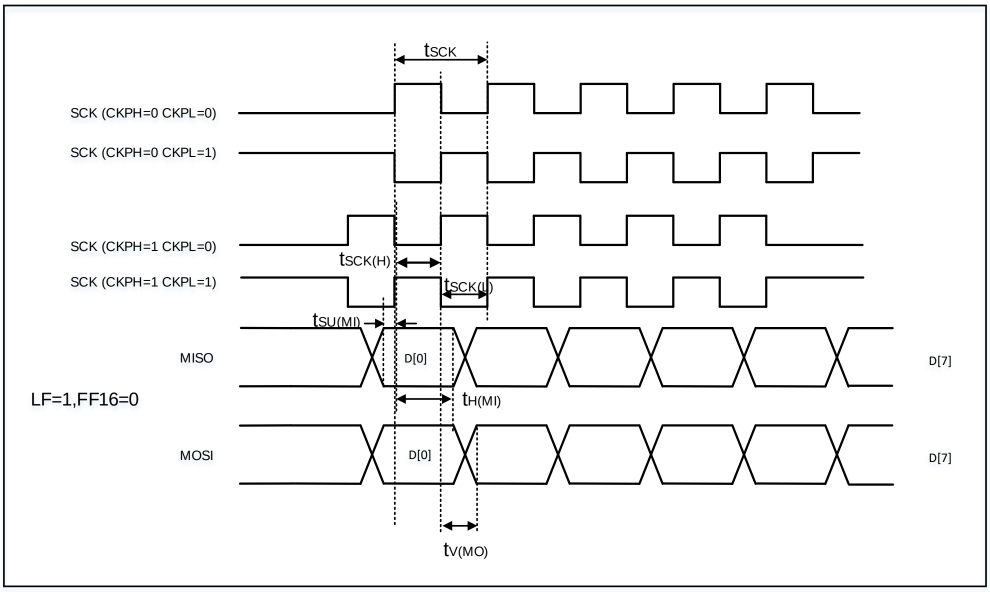
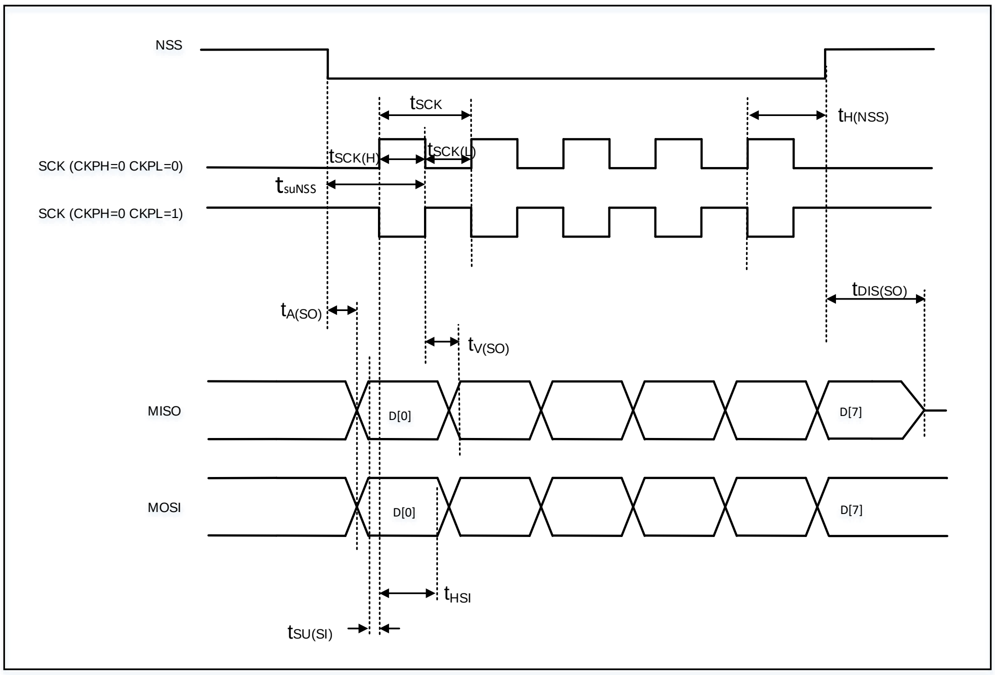


Figure 4-8. SPI timing diagram - slave mode



4.18. I2S characteristics

Table 4-35. I2S characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 16 bits, Audio frequency = 96 kHz)	—	3.078	—	MHz
		Slave mode	—	10	—	
t_H	Clock high time	—	—	162	—	ns
t_L	Clock low time		—	163	—	ns
$t_{V(WS)}$	WS valid time	Master mode	—	2	—	ns
$t_{H(WS)}$	WS hold time	Master mode	—	2	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	—	—	ns
$DuCy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	0	—	—	ns
$t_{su(SD\_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	1	—	—	ns
$t_{H(SD\_SR)}$		Slave receiver	3	—	—	ns
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	12	—	ns
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter	—	10	—	ns

		(after enable edge)				
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	10	—	ns
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	—	7	—	ns

(1) Guaranteed by design, not tested in production.
(2) Based on characterization, not tested in production.

Figure 4-9. I2S timing diagram - master mode

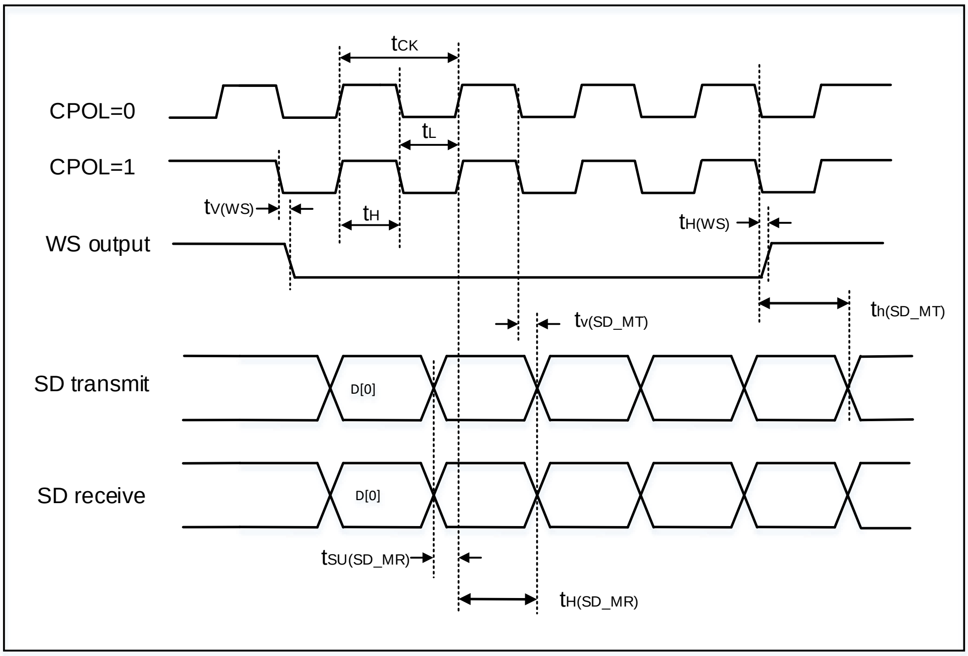
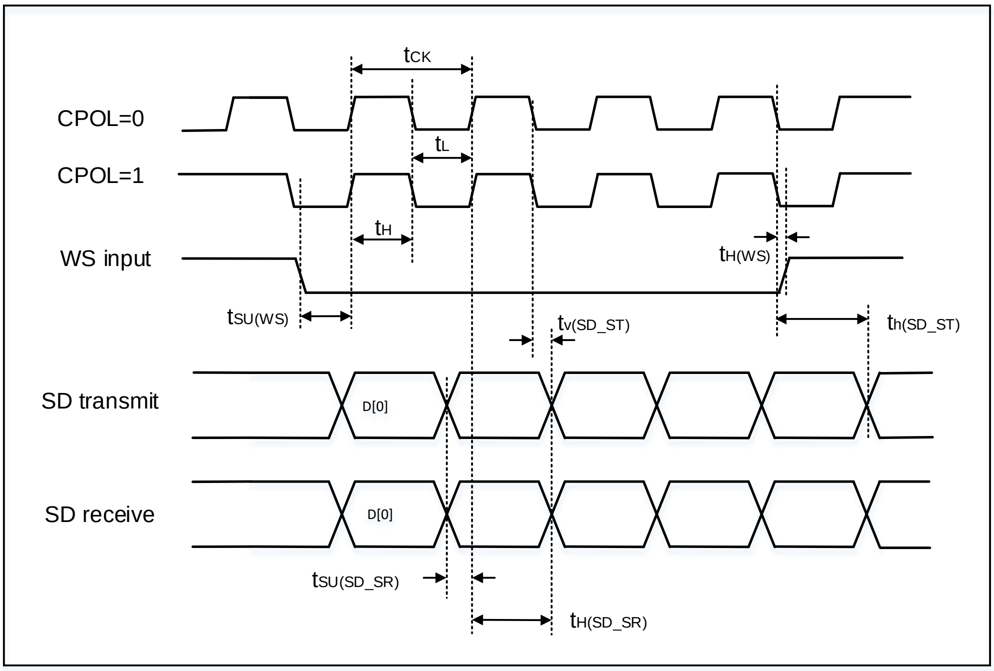


Figure 4-10. I2S timing diagram - slave mode



4.19. USART characteristics

Table 4-36. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 120 MHz	—	—	60	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 120 MHz	7.5	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 120 MHz	7.5	—	—	ns

(1) Guaranteed by design, not tested in production.

4.20. USBFS characteristics

Table 4-37. USBFS start up time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USBFS startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 4-38. USBFS DC electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
Input levels(1)	V_{DD}	USBFS operating voltage	—	3	—	3.6	V
	V_{DI}	Differential input sensitivity	—	0.2	—	—	
	V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	—	2.5	
	V_{SE}	Single ended receiver threshold	—	1.3	—	2.0	
Output levels (2)	V_{OL}	Static output level low	R_L of 1.0 kΩ to 3.6 V	—	0.064	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to VSS	2.8	3.3	3.6	
R_{PD}(2)		PA11, PA12(USB_DM/DP)	$V_{IN} = V_{DD}$	17	20.574	24	kΩ
		PA9(USB_VBUS)		0.65	—	2.0	
R_{PU}(2)		PA11, PA12(USB_DM/DP)	$V_{IN} = V_{SS}$	1.5	1.585	2.1	
		PA9(USB_VBUS)		0.25	0.326	0.55	

(1) Guaranteed by design, not tested in production.

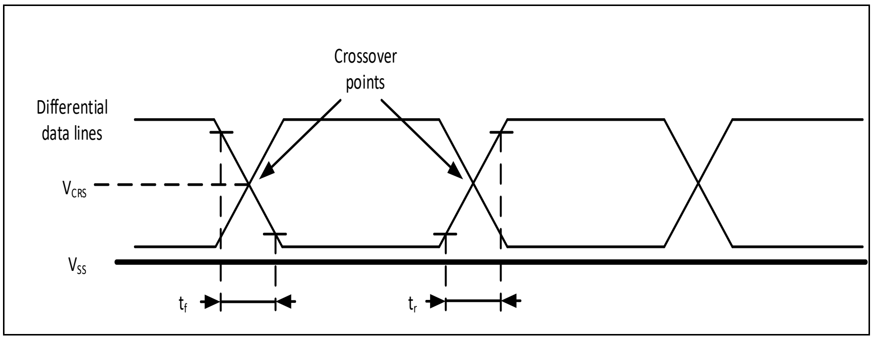
(2) Based on characterization, not tested in production.

Table 4-39. USBFS electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Rise time	C_L = 50 pF	4	—	20	ns
t_F	Fall time	C_L = 50 pF	4	—	20	ns
t_{RFM}	Rise/fall time matching	t_R/t_F	90	—	110	%
V_{CRS}	Output signal crossover voltage	—	1.3	—	2.0	V

(1) Guaranteed by design, not tested in production.

Figure 4-11. USBFS timings: definition of data signal rise and fall time



4.21. EXMC characteristics

Table 4-40. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	40.5	42.5	ns
$t_{V(NOE\_NE)}$	EXMC_NEx low to EXMC_NOE low	0	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	40.5	42.5	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{su(DATA\_NE)}$	Data to EXMC_NEx high setup time	32.2	—	ns
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	32.2	—	ns

$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	7.3	9.3	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK} = 120 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-41. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	23.9	25.9	ns
$t_{V(NWE\_NE)}$	EXMC_NEx low to EXMC_NWE low	7.3	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	7.3	9.3	ns
$t_{h(NE\_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	7.3	9.3	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	7.3	9.3	ns
$t_{h(AD\_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	15.6	—	ns
$t_{h(A\_NWE)}$	Address hold time after EXMC_NWE high	7.3	—	ns
$t_{h(BL\_NWE)}$	EXMC_BL hold time after EXMC_NWE high	7.3	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA\_NADV)}$	EXMC_NADV high to DATA valid	0	—	ns
$t_{h(DATA\_NWE)}$	Data hold time after EXMC_NWE high	7.3	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK} = 120 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-42. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	57.1	59.1	ns
$t_{V(NOE\_NE)}$	EXMC_NEx low to EXMC_NOE low	23.9	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	32.2	34.2	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(A\_NOE)}$	Address hold time after EXMC_NOE high	0	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{h(BL\_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	—	ns
$t_{su(DATA\_NE)}$	Data to EXMC_NEx high setup time	33.2	—	ns
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	33.2	—	ns
$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	7.3	9.3	ns
$T_{h(AD\_NADV)}$	EXMC_AD(adress) valid hold time after	7.3	9.3	ns

	EXMC_NADV high			

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK} = 120 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-43. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	40.5	42.5	ns
$t_{V(NWE\_NE)}$	EXMC_NEx low to EXMC_NWE low	7.3	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	23.9	25.9	ns
$t_{h(NE\_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	7.3	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	7.3	9.3	ns
$t_{h(AD\_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	7.3	—	ns
$t_{h(A\_NWE)}$	Address hold time after EXMC_NWE high	7.3	—	ns
$t_{h(BL\_NWE)}$	EXMC_BL hold time after EXMC_NWE high	7.3	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA\_NADV)}$	EXMC_NADV high to DATA valid	7.3	—	ns
$t_{h(DATA\_NWE)}$	Data hold time after EXMC_NWE high	7.3	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK} = 120 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime =1.

Table 4-44. Synchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	33.2	—	ns
$t_{d(CLKL\text{-}NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH\text{-}NExH)}$	EXMC_CLK high to EXMC_NEx high	15.6	—	ns
$t_{d(CLKL\text{-}NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL\text{-}NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL\text{-}AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH\text{-}AIV)}$	EXMC_CLK high to EXMC_Ax invalid	15.6	—	ns
$t_{d(CLKL\text{-}NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH\text{-}NOEH)}$	EXMC_CLK high to EXMC_NOE high	15.6	—	ns
$t_{d(CLKL\text{-}ADV)}$	EXMC_CLK low to EXMC_AD valid	0	—	ns
$t_{d(CLKL\text{-}ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK} = 120 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-45. Synchronous multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	33.2	—	ns

$t_{d(CLKL\text{-}NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH\text{-}NExH)}$	EXMC_CLK high to EXMC_NEx high	15.6	—	ns
$t_{d(CLKL\text{-}NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL\text{-}NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL\text{-}AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH\text{-}AIV)}$	EXMC_CLK high to EXMC_Ax invalid	15.6	—	ns
$t_{d(CLKL\text{-}NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH\text{-}NWEH)}$	EXMC_CLK high to EXMC_NWE high	15.6	—	ns
$t_{d(CLKL\text{-}ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns
$t_{d(CLKL\text{-}DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL\text{-}NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: f_{HCLK} = 120 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-46. Synchronous non-multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	33.2	—	ns
$t_{d(CLKL\text{-}NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH\text{-}NExH)}$	EXMC_CLK high to EXMC_NEx high	15.6	—	ns
$t_{d(CLKL\text{-}NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL\text{-}NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL\text{-}AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH\text{-}AIV)}$	EXMC_CLK high to EXMC_Ax invalid	15.6	—	ns
$t_{d(CLKL\text{-}NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH\text{-}NOEH)}$	EXMC_CLK high to EXMC_NOE high	15.6	—	ns

(1) C_L = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: f_{HCLK} = 120 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-47. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	33.2	—	ns
$t_{d(CLKL\text{-}NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH\text{-}NExH)}$	EXMC_CLK high to EXMC_NEx high	15.6	—	ns
$t_{d(CLKL\text{-}NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL\text{-}NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL\text{-}AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH\text{-}AIV)}$	EXMC_CLK high to EXMC_Ax invalid	15.6	—	ns
$t_{d(CLKL\text{-}NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH\text{-}NWEH)}$	EXMC_CLK high to EXMC_NWE high	15.6	—	ns
$t_{d(CLKL\text{-}DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL\text{-}NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: f_{HCLK} = 120 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3(EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

4.22. TIMER characteristics

Table 4-48. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 120 MHz	8.4	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 120 MHz	0	60	MHz
RES	Timer resolution	—	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 120 MHz	0.0084	546	µs
t_{MAX_COUNT}	Maximum possible count	—	—	65536x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 120 MHz	—	35.7	s

(1) Guaranteed by design, not tested in production.

4.23. WDGT characteristics

Table 4-49. FWDGT min/max timeout period at 40 kHz (IRC40K)(1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.025	409.525	ms
1/8	001	0.025	819.025	
1/16	010	0.025	1638.025	
1/32	011	0.025	3276.025	
1/64	100	0.025	6552.025	
1/128	101	0.025	13104.025	
1/256	110 or 111	0.025	26208.025	

(1) Guaranteed by design, not tested in production.

Table 4-50. WWDGT min-max timeout value at 60 MHz (f_{PCLK1})(1)

Prescaler divider	PSC[1:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	68.2	µs	4.3	ms
1/2	01	136.4		8.6	
1/4	10	272.8		17.2	
1/8	11	545.6		34.4	

(1) Guaranteed by design, not tested in production.

4.24. Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 ℃.

5. Package information

5.1. LQFP100 package outline dimensions

Figure 5-1. LQFP100 package outline

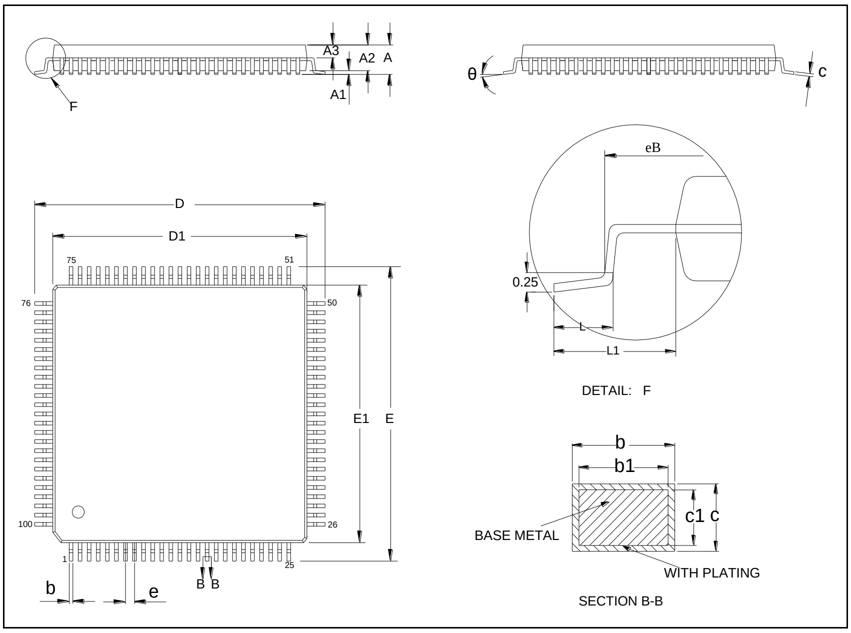
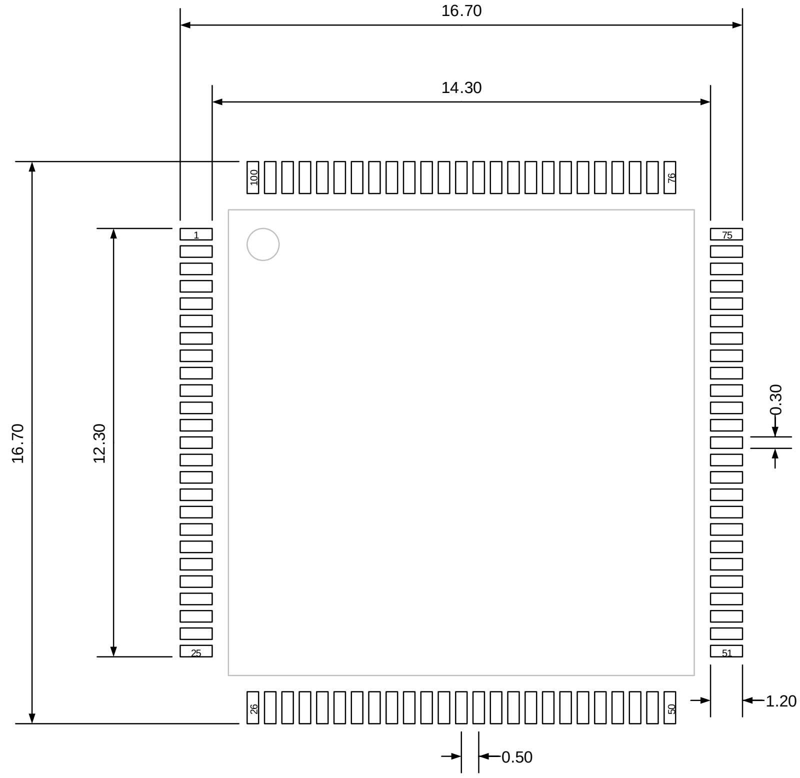


Table 5-1. LQFP100 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	—	0.50	—
eB	15.05	—	15.35
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-2. LQFP100 recommended footprint



(Original dimensions are in millimeters)

5.2. LQFP64 package outline dimensions

Figure 5-3. LQFP64 package outline

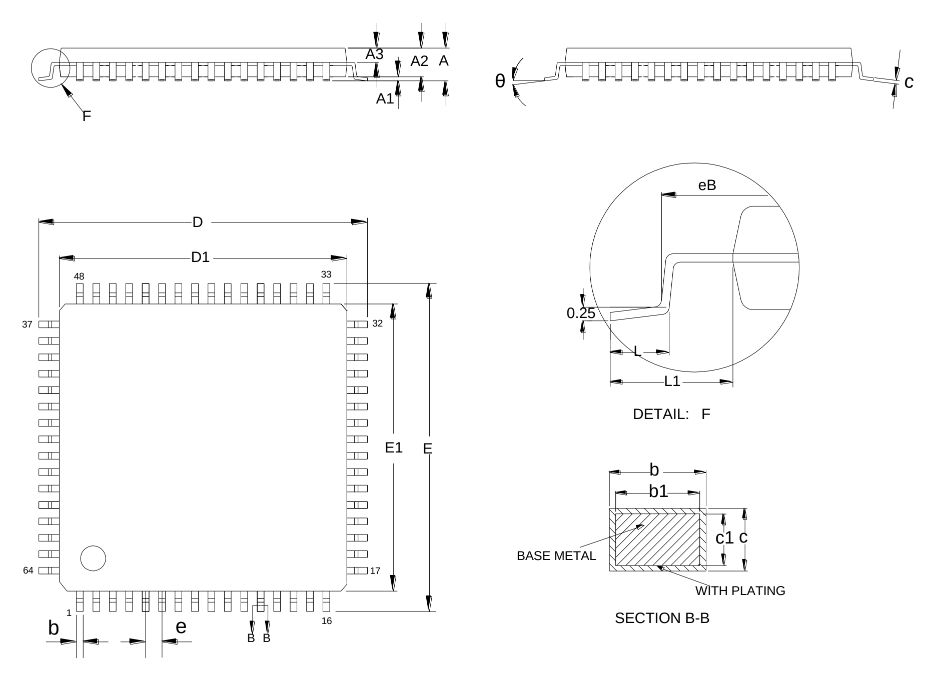
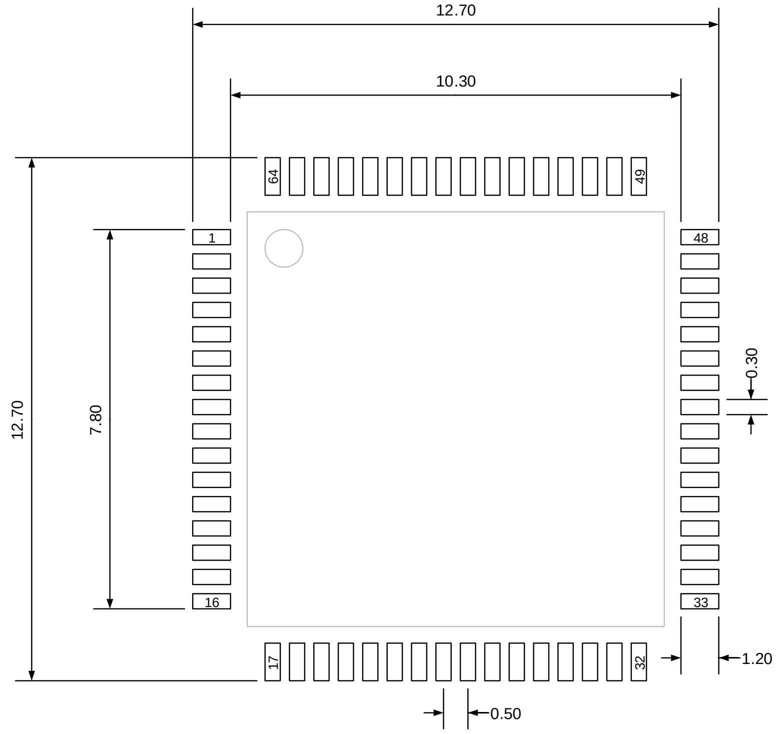


Table 5-2. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	—	0.50	—
eB	11.25	—	11.45
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-4. LQFP64 recommended footprint



(Original dimensions are in millimeters)

5.3. LQFP48 package outline dimensions

Figure 5-5. LQFP48 package outline

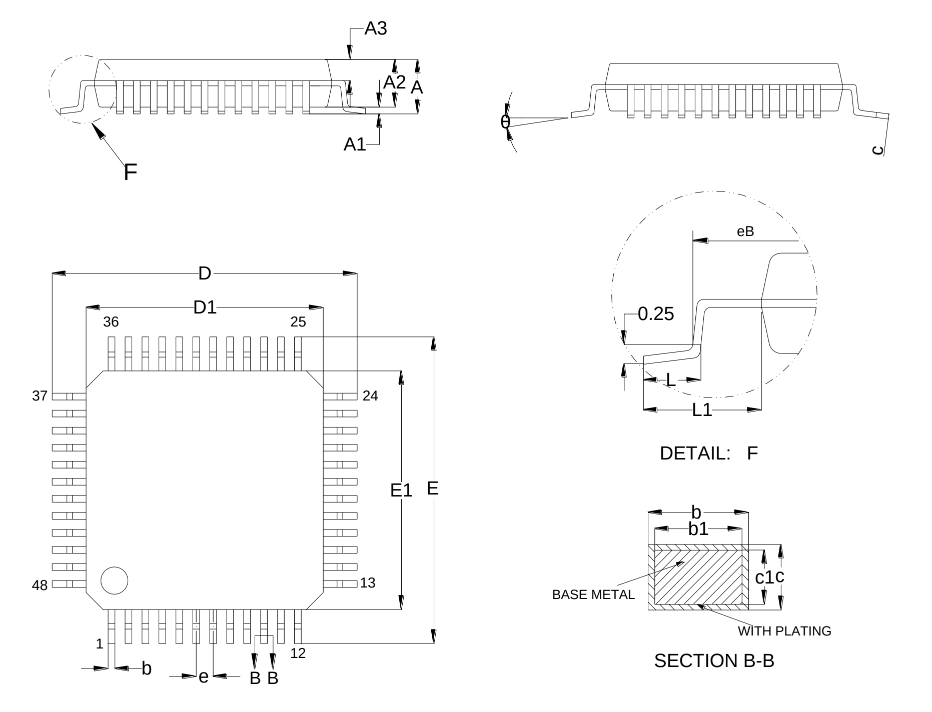
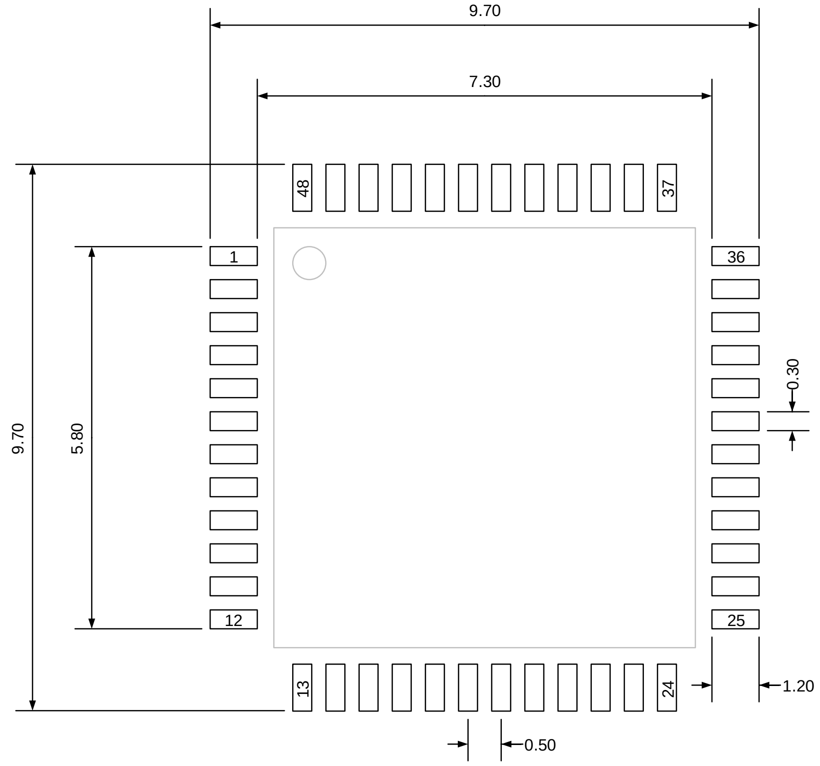


Table 5-3. LQFP48 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.50	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-6. LQFP48 recommended footprint



(Original dimensions are in millimeters)

5.4. QFN36 package outline dimensions

Figure 5-7. QFN36 package outline

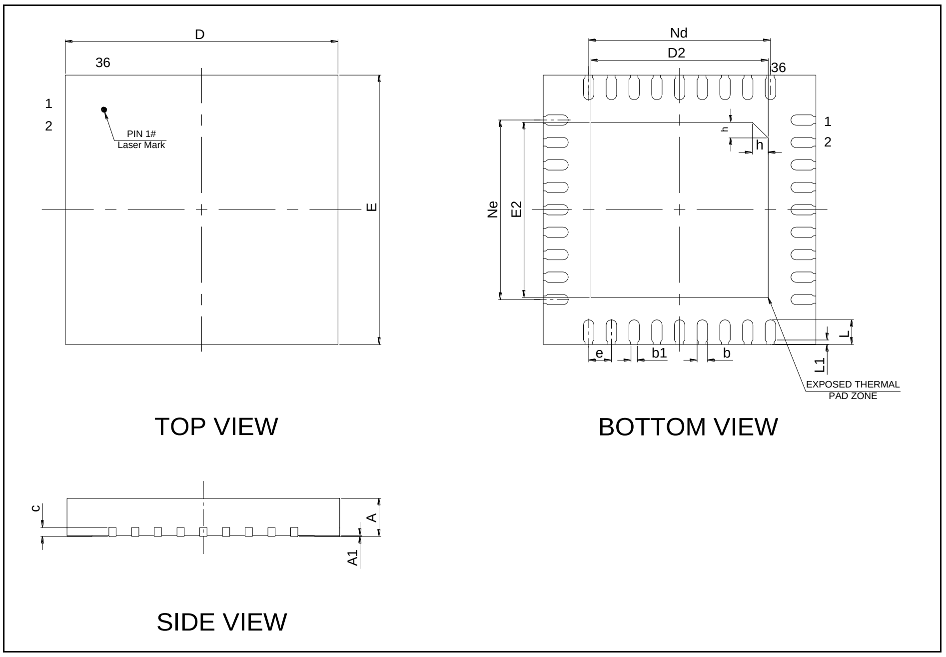
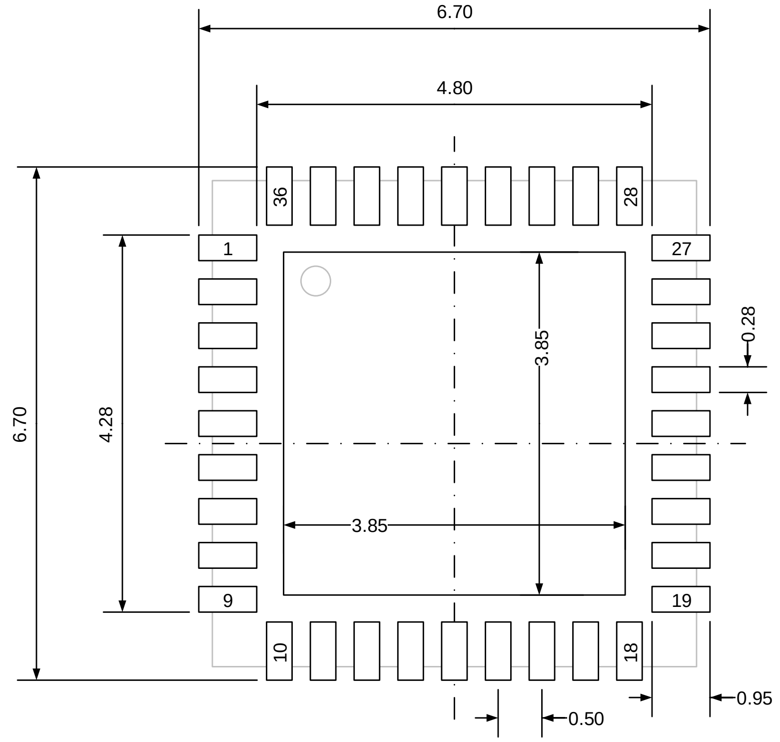


Table 5-4. QFN36 package dimensions

Symbol	Min	Typ	Max
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.18	0.23	0.30
b1	—	0.16	—
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	3.80	3.90	4.00
E	5.90	6.00	6.10
E2	3.80	3.90	4.00
e	—	0.50	—
h	0.30	0.35	0.40
L	0.50	0.55	0.60
L1	—	0.10	—
Nd	3.95	4.00	4.05
Ne	3.95	4.00	4.05

(Original dimensions are in millimeters)

Figure 5-8. QFN36 recommended footprint



(Original dimensions are in millimeters)

5.5. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “θ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \tag{5-1}$$

$$\theta_{JB}=(T_J-T_B)/P_D \tag{5-2}$$

$$\theta_{JC}=(T_J-T_C)/P_D \tag{5-3}$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-5. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
Θ_{JA}	Natural convection, 2S2P PCB	LQFP100	49.18	°C/W
		LQFP64	54.57	
		LQFP48	69.64	
		QFN36	36.82	
Θ_{JB}	Cold plate, 2S2P PCB	LQFP100	22.70	°C/W
		LQFP64	35.08	
		LQFP48	43.16	

Symbol	Condition	Package	Value	Unit
		QFN36	9.79	
Θ_{JC}	Cold plate, 2S2P PCB	LQFP100	12.52	°C/W
		LQFP64	18.11	
		LQFP48	25.36	
		QFN36	13.31	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP100	32.85	°C/W
		LQFP64	35.41	
		LQFP48	47.75	
		QFN36	9.87	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP100	0.53	°C/W
		LQFP64	1.10	
		LQFP48	2.45	
		QFN36	0.43	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32E103xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32E103VBT6	128	LQFP100	Green	Industrial -40 °C to +85 °C
GD32E103V8T6	64	LQFP100	Green	Industrial -40 °C to +85 °C
GD32E103RBT6	128	LQFP64	Green	Industrial -40 °C to +85 °C
GD32E103R8T6	64	LQFP64	Green	Industrial -40 °C to +85 °C
GD32E103CBT6	128	LQFP48	Green	Industrial -40 °C to +85 °C
GD32E103C8T6	64	LQFP48	Green	Industrial -40 °C to +85 °C
GD32E103TBU6	128	QFN36	Green	Industrial -40 °C to +85 °C
GD32E103T8U6	64	QFN36	Green	Industrial -40 °C to +85 °C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Dec. 26, 2017
1.1	Modify section 2.6 Pin definitions	Oct. 29, 2018
1.2	Repair history accumulation error	Dec. 12, 2018
1.3	Modify section 5.1 LQFP package outline dimensions	Apr. 22, 2019
1.4	Modify section 2.6 Pin definitions	Jun. 26, 2019
1.5	Remove redundant pin function in LQFP48 and QFN36 package. Add functional description of PD0 and PD1 to the packages below 100pin. Update electrical characteristics.	Mar. 6, 2020
1.6	Modify some function definition of TIMER pins and other description changes.	Sep. 11, 2020
1.7	1. Modify the function definition of PB15(TIMER11_CH1). 2. T_{STG} range changed from -55 - +150 °C to -65 - 150 °C in section 4.1. 3. Modify the description of Supply current (Deep-Sleep mode) in section 4.3. 4. Add I2C timing diagram, modify SPI timing diagram and add I2S timing diagram in section 4.16, 4.17, 4.18. 5. Adjust the number of modules and delete CAN.	Jan. 4, 2021
1.8	Electrical characteristics update.	Feb. 25, 2021
1.9	1. Update I2C timing diagram and proofread WDGT min-max timeout value. VIN maximum value cannot exceed 6.5 V, changed to 5.5V in Table 4-1. 2. Update LQFP100_14X14, LQFP64_10X10, LQFP48_7X7 and QFN36-6X6 package outline	Dec. 13, 2021

	and package dimensions, increase recommended footprint, increase thermal resistance description section and parameter section content. 3. Change the LQFP176 and LQFP144 POD diagrams, and add eB parameters to the POD parameters in packages below LQFP100 in section ***5.1*** and delete the temperature information in the Condition in the thermal resistance in section ***5***. 4. Modify ***Table 4-1*** and ***Table 4-11***. Delete ETM support.	

Important Notice