

DDR4 SDRAM UDIMM

Based on 16Gb A-die

HMAA2GU6AJR8N
HMAA4GU6AJR8N
HMAA4GU7AJR8N

***SK hynix reserves the right to change products or specifications without notice.**

Revision History

| Revision No. | History | Draft Date | Remark |
|--------------|---|------------|--------|
| 0.1 | Initial Release | Mar.2019 | |
| 0.2 | Add ECC-UD Specification | Apr.2019 | |
| 1.0 | Define IDD/IPP Specification | Jun.2019 | |
| 1.1 | Current IDD/IPP Specification Add 1Rx8 nECC-UD Specification | Aug.2019 | |

Description

SK hynix Unbuffered DDR4 SDRAM DIMMs (Unbuffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Unbuffered SDRAM DIMMs are intended for use as main memory when installed in systems such as PCs and workstations.

Features

- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP - 2.5V (2.375V to 2.75V)
- VDDSPD=2.25V to 3.6V
- Functionality and operations comply with the DDR4 SDRAM datasheet
- 16 internal banks
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- Data transfer rates: PC4-3200, PC4-2933, PC4-2666, PC4-2400, PC4-2133, PC4-1866, PC4-1600
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- Supports ECC error correction and detection
- On-Die Termination (ODT)
- Temperature sensor with integrated SPD for ECC UDIMM
- This product is in compliance with the RoHS directive.
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available

Ordering Information

| Part Number | Density | Organization | Component Composition | # of ranks |
|--------------------------|---------|--------------|-----------------------|------------|
| HMAA2GU6AJR8N - VK/WM/XN | 16GB | 2Gx64 | 2Gx8(H5ANAG8NAJR)*8 | 1 |
| HMAA4GU6AJR8N - VK/WM/XN | 32GB | 4Gx64 | 2Gx8(H5ANAG8NAJR)*16 | 2 |
| HMAA4GU7AJR8N - VK/WM/XN | 32GB | 4Gx72 | 2Gx8(H5ANAG8NAJR)*18 | 2 |

Key Parameters

| MT/s | Grade | tCK (ns) | CAS Latency (tCK) | tRCD (ns) | tRP (ns) | tRAS (ns) | tRC (ns) | CL-tRCD-tRP |
|------------------|-------|----------|-------------------|-------------------|-------------------|-----------|-------------------|-------------|
| DDR4-1600 | -PB | 1.25 | 11 | 13.75 (13.50)* | 13.75 (13.50)* | 35 | 48.75 (48.50)* | 11-11-11 |
| DDR4-1866 | -RD | 1.071 | 13 | 13.92 (13.50)* | 13.92 (13.50)* | 34 | 47.92 (47.50)* | 13-13-13 |
| DDR4-2133 | -TF | 0.937 | 15 | 14.06 (13.50)* | 14.06 (13.50)* | 33 | 47.06 (46.50)* | 15-15-15 |
| DDR4-2400 | -UH | 0.833 | 17 | 14.16 (13.75)* | 14.16 (13.75)* | 32 | 46.16 (45.75)* | 17-17-17 |
| DDR4-2666 | -VK | 0.75 | 19 | 14.25 (13.75)* | 14.25 (13.75)* | 32 | 46.25 (45.75)* | 19-19-19 |
| DDR4-2933 | -WM | 0.682 | 21 | 14.32 (13.75)* | 14.32 (13.75)* | 32 | 46.32 (45.75)* | 21-21-21 |
| DDR4-3200 | -XN | 0.625 | 22 | 13.75 | 13.75 | 32 | 47.0 | 22-22-22 |

*SK hynix DRAM devices support optional downbinning to CL21, CL19, CL17, CL15, CL13 and CL11. SPD setting is programmed to match.

Address Table

| | | 16GB(1RX8) | 32GB(2RX8) |
|-----------------------|-----------------------------|------------|------------|
| Bank Address | # of Bank Groups | 4 | 4 |
| | BG Address | BG0~BG1 | BG0~BG1 |
| | Bank Address in a BG | BA0~BA1 | BA0~BA1 |
| Row Address | | A0~A16 | A0~A16 |
| Column Address | | A0~ A9 | A0~ A9 |
| Page size | | 1KB | 1KB |

Pin Descriptions

| Pin Name | Description | Pin Name | Description |
|------------------------------------|--|------------|---|
| A0-A17 ¹ | SDRAM address bus | SCL | I ² C serial bus clock for SPD-TSE |
| BA0, BA1 | SDRAM bank select | SDA | I ² C serial bus line for SPD-TSE |
| BG0, BG1 | SDRAM bank group select | SA0-SA2 | I ² C slave address select for SPD-TSE |
| RAS_n ² | SDRAM row address strobe | PARITY | SDRAM parity input |
| CAS_n ³ | SDRAM column address strobe | VDD | SDRAM I/OO and core power supply |
| WE_n ⁴ | SDRAM write enable | C0, C1, C2 | Chip ID lines |
| CS0_n, CS1_n, | DIMM Rank Select Lines | 12V | Optional power Supply on socket but not used on UDIMM |
| CKE0, CEK1 | SDRAM clock enable lines input | VREFCA | SDRAM command/address reference supply |
| ODT0, ODT1 | SDRAM on-die termination control lines input | VSS | Power supply return (ground) |
| ACT_n | SDRAM activate | VDDSPD | Serial SPD-TSE positive power supply |
| DQ0-DQ63 | DIMM memory data bus | ALERT_n | SDRAM ALERT_n output |
| CB0-CB7 | DIMM ECC check bits | VPP | SDRAM Supply |
| TDQS0_t-TDQS8_t TDQS0_c-TDQS8_c | Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs. | | |
| DQS0_t-DQS8_t | SDRAM data strobes (positive line of differential pair) | | |
| DQS0_c-DQS8_c | SDRAM data strobes (negative line of differential pair) | RESET_n | Set DRAMs to a Known State |
| DM0_n-DM8_n, DBI0_n-DBI8_n | SDRAM data masks/data bus inersion (x8-based x72 DIMMs) | EVENT_n | SPD signals a thermal event has occurred |
| CK0_t, CK1_t | SDRAM clock (positive line of differential pair) | VTT | SDRAM I/O termination supply |
| CK0_c, CK1_c | SDRAM clock (positive line of differential pair) | RFU | Reserved for future use |

1. Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs, this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Input/Output Functional Descriptions

| Symbol | Type | Function |
|---|------------------|--|
| CK0_t, CK0_c, CK1_t, CK1_c | Input | Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c. |
| CKE0, CKE1 | Input | Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh. |
| CS0_n, CS1_n, CS2_n, CS3_n | Input | Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS2_n and CS_3_n are not used on UDIMMs. |
| C0, C1, C2 | Input | Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code. Not used on UDIMMs. |
| ODT0, ODT1 | Input | On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t,NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM. |
| ACT_n | Input | Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14. |
| RAS_n/A16, CAS_n/A15, WE_n/A14 | Input | Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15, and A14. But for non-activation command with ACT_n High, these are Command pins for Read, Write, and other commands defined in command truth table. |
| DM_n/DBI_n/ TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n) | Input/ Output | Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. TDQS is not valid for UDIMMs. |

| Symbol | Type | Function |
|--|---------------|--|
| BG0, BG1 | Input | Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/x8 SDRAM configurations have BG0 and BG1. x16 based SDRAMs only have BG0. |
| BA0, BA1 | Input | Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle. |
| A0 - A17 | Input | Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 SDRAM configuration. |
| A10 / AP | Input | Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. |
| A12 / BC_n | Input | Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details. |
| RESET_n | CMOS Input | Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. |
| DQ | Input/ Output | Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. |
| DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c | Input/ Output | Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended. |
| TDQS_t, TDQS_c | Output | Termination Data Strobe: TDQS_t/TDQS_c are not valid for UDIMMs. |
| PARITY | Input | Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW. |

| Symbol | Type | Function |
|------------------|--------|--|
| ALERT_n | Output | Alert: It has multiple functions, such as CRC error flag, Command and Address Parity error flag, as an Output signal. If there is an error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is an error in Command Address Parity Check, then ALERT_n goes LOW for a relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input. Using this signal or not is dependent on the system. |
| RFU | | Reserved for Future Use. No on DIMM electrical connection is present. |
| NC | | No Connect: No on DIMM electrical connection is present. |
| VDD ¹ | Supply | Power Supply: 1.2 V +/- 0.06 V |
| VSS | Supply | Ground |
| VPP | Supply | DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max) |
| VTT ² | Supply | Power Supply for termination of Address, Command and Control, VDD/2. |
| 12V | Supply | 12V supply not used on UDIMMs. |
| VDDSDP | Supply | Power supply used to power the I2C bus on the SPD-TSE |
| VREFCA | Supply | Reference voltage for CA |

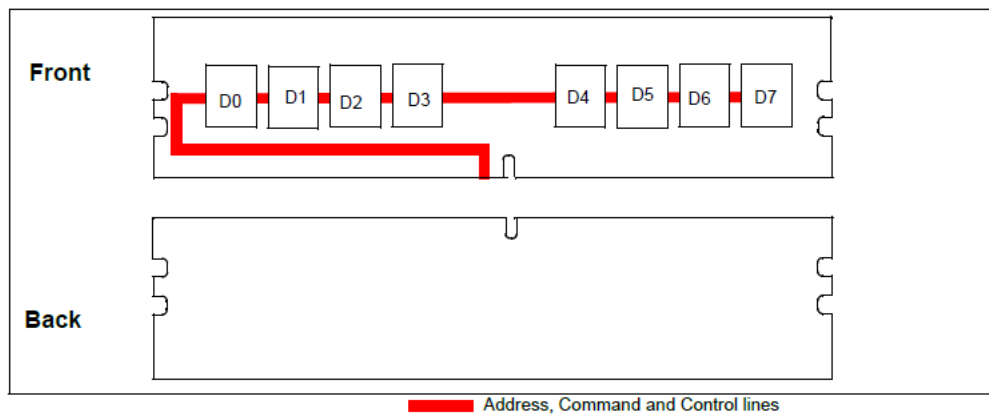
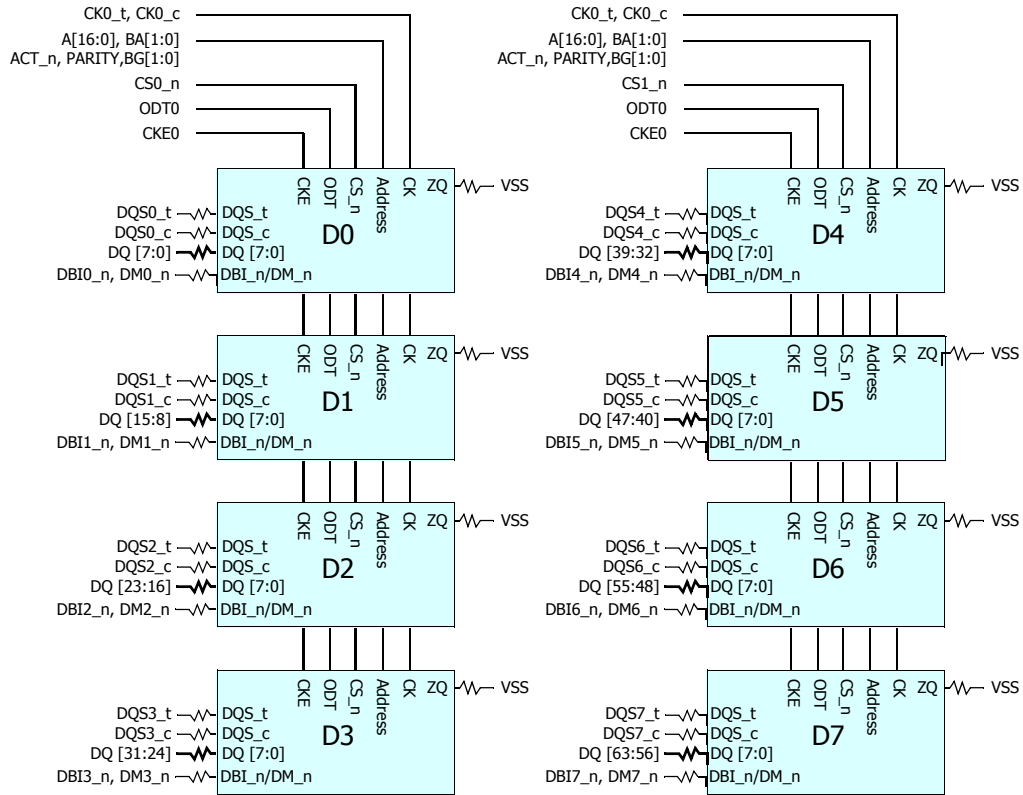
Pin Assignments

| Pin | Front Side Pin Label | Pin | Back Side Pin Label | Pin | Front Side Pin Label | Pin | Back Side Pin Label |
|-----|----------------------|-----|---------------------|-----|----------------------|-----|---------------------|
| 1 | NC | 145 | NC | 74 | CK0_t | 218 | CK1_t |
| 2 | VSS | 146 | VREFCA | 75 | CK0_c | 219 | CK1_c |
| 3 | DQ4 | 147 | VSS | 76 | VDD | 220 | VDD |
| 4 | VSS | 148 | DQ5 | 77 | VTT | 221 | VTT |
| 5 | DQ0 | 149 | VSS | KEY | | | |
| 6 | VSS | 150 | DQ1 | | | | |
| 7 | DM0_n, DBI0_n, NC | 151 | VSS | 78 | EVENT_n | 222 | PARITY |
| 8 | NC | 152 | DQS0_c | 79 | A0 | 223 | VDD |
| 9 | VSS | 153 | DQS0_t | 80 | VDD | 224 | BA1 |
| 10 | DQ6 | 154 | VSS | 81 | BA0 | 225 | A10/AP |
| 11 | VSS | 155 | DQ7 | 82 | RAS_n/A16 | 226 | VDD |
| 12 | DQ2 | 156 | VSS | 83 | VDD | 227 | RFU |
| 13 | VSS | 157 | DQ3 | 84 | CS0_n | 228 | WE_n/A14 |
| 14 | DQ12 | 158 | VSS | 85 | VDD | 229 | VDD |
| 15 | VSS | 159 | DQ13 | 86 | CAS_n/A15 | 230 | NC |
| 16 | DQ8 | 160 | VSS | 87 | ODT0 | 231 | VDD |
| 17 | VSS | 161 | DQ9 | 88 | VDD | 232 | A13 |
| 18 | DM1_n, DBI1_n, NC | 162 | VSS | 89 | CS1_n | 233 | VDD |
| 19 | NC | 163 | DQS1_c | 90 | VDD | 234 | NC |
| 20 | VSS | 164 | DQS1_t | 91 | ODT1 | 235 | NC |
| 21 | DQ14 | 165 | VSS | 92 | VDD | 236 | VDD |
| 22 | VSS | 166 | DQ15 | 93 | NC | 237 | NC |
| 23 | DQ10 | 167 | VSS | 94 | VSS | 238 | SA2 |
| 24 | VSS | 168 | DQ11 | 95 | DQ36 | 239 | VSS |
| 25 | DQ20 | 169 | VSS | 96 | VSS | 240 | DQ37 |
| 26 | VSS | 170 | DQ21 | 97 | DQ32 | 241 | VSS |
| 27 | DQ16 | 171 | VSS | 98 | VSS | 242 | DQ33 |
| 28 | VSS | 172 | DQ17 | 99 | DM4_n, DBI4_n, NC | 243 | VSS |
| 29 | DM2_n, DBI2_n, NC | 173 | VSS | 100 | NC | 244 | DQS4_c |
| 30 | NC | 174 | DQS2_c | 101 | VSS | 245 | DQS4_t |
| 31 | VSS | 175 | DQS2_t | 102 | DQ38 | 246 | VSS |
| 32 | DQ22 | 176 | VSS | 103 | VSS | 247 | DQ39 |
| 33 | VSS | 177 | DQ23 | 104 | DQ34 | 248 | VSS |
| 34 | DQ18 | 178 | VSS | 105 | VSS | 249 | DQ35 |
| 35 | VSS | 179 | DQ19 | 106 | DQ44 | 250 | VSS |
| 36 | DQ28 | 180 | VSS | 107 | VSS | 251 | DQ45 |
| 37 | VSS | 181 | DQ29 | 108 | DQ40 | 252 | VSS |
| 38 | DQ24 | 182 | VSS | 109 | VSS | 253 | DQ41 |

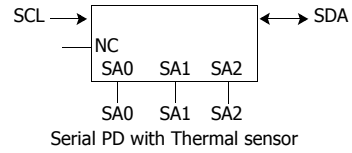
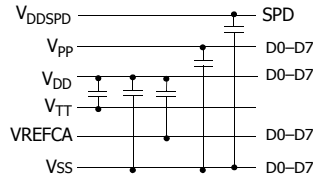
| Pin | Front Side Pin Label | Pin | Back Side Pin Label | Pin | Front Side Pin Label | Pin | Back Side Pin Label |
|-----|----------------------|-----|---------------------|-----|----------------------|-----|---------------------|
| 39 | VSS | 183 | DQ25 | 110 | DM5_n, DBI5_n, NC | 254 | VSS |
| 40 | DM3_n, DBI3_n, NC | 184 | VSS | 111 | NC | 255 | DQS5_c |
| 41 | NC | 185 | DQS3_c | 112 | VSS | 256 | DQS5_t |
| 42 | VSS | 186 | DQS3_t | 113 | DQ46 | 257 | VSS |
| 43 | DQ30 | 187 | VSS | 114 | VSS | 258 | DQ47 |
| 44 | VSS | 188 | DQ31 | 115 | DQ42 | 259 | VSS |
| 45 | DQ26 | 189 | VSS | 116 | VSS | 260 | DQ43 |
| 46 | VSS | 190 | DQ27 | 117 | DQ52 | 261 | VSS |
| 47 | CB4, NC | 191 | VSS | 118 | VSS | 262 | DQ53 |
| 48 | VSS | 192 | CB5, NC | 119 | DQ48 | 263 | VSS |
| 49 | CB0, NC | 193 | VSS | 120 | VSS | 264 | DQ49 |
| 50 | VSS | 194 | CB1, NC | 121 | DM6_n, DBI6_n, NC | 265 | VSS |
| 51 | DM8_n, DBI8_n, NC | 195 | VSS | 122 | NC | 266 | DQS6_c |
| 52 | NC | 196 | DQS8_c | 123 | VSS | 267 | DQS6_t |
| 53 | VSS | 197 | DQS8_t | 124 | DQ54 | 268 | VSS |
| 54 | CB6, NC | 198 | VSS | 125 | VSS | 269 | DQ55 |
| 55 | VSS | 199 | CB7, NC | 126 | DQ50 | 270 | VSS |
| 56 | CB2, NC | 200 | VSS | 127 | VSS | 271 | DQ51 |
| 57 | VSS | 201 | CB3, NC | 128 | DQ60 | 272 | VSS |
| 58 | RESET_n | 202 | VSS | 129 | VSS | 273 | DQ61 |
| 59 | VDD | 203 | CKE1 | 130 | DQ56 | 274 | VSS |
| 60 | CKE0 | 204 | VDD | 131 | VSS | 275 | DQ57 |
| 61 | VDD | 205 | RFU | 132 | DM7_n, DBI7_n, NC | 276 | VSS |
| 62 | ACT_n | 206 | VDD | 133 | NC | 277 | DQS7_c |
| 63 | BG0 | 207 | BG1 | 134 | VSS | 278 | DQS7_t |
| 64 | VDD | 208 | ALERT_n | 135 | DQ62 | 279 | VSS |
| 65 | A12/BC_n | 209 | VDD | 136 | VSS | 280 | DQ63 |
| 66 | A9 | 210 | A11 | 137 | DQ58 | 281 | VSS |
| 67 | VDD | 211 | A7 | 138 | VSS | 282 | DQ59 |
| 68 | A8 | 213 | VDD | 139 | SA0 | 283 | VSS |
| 69 | A6 | 214 | A5 | 140 | SA1 | 284 | VDDSPD |
| 70 | VDD | 215 | A4 | 141 | SCL | 285 | SDA |
| 71 | A3 | 215 | VDD | 142 | VPP | 286 | VPP |
| 72 | A1 | 216 | A2 | 143 | VPP | 287 | VPP |
| 73 | VDD | 217 | VDD | 144 | RFU | 288 | VPP |

Functional Block Diagram

16GB, 2Gx64 Module(1Rank of x8) - page1



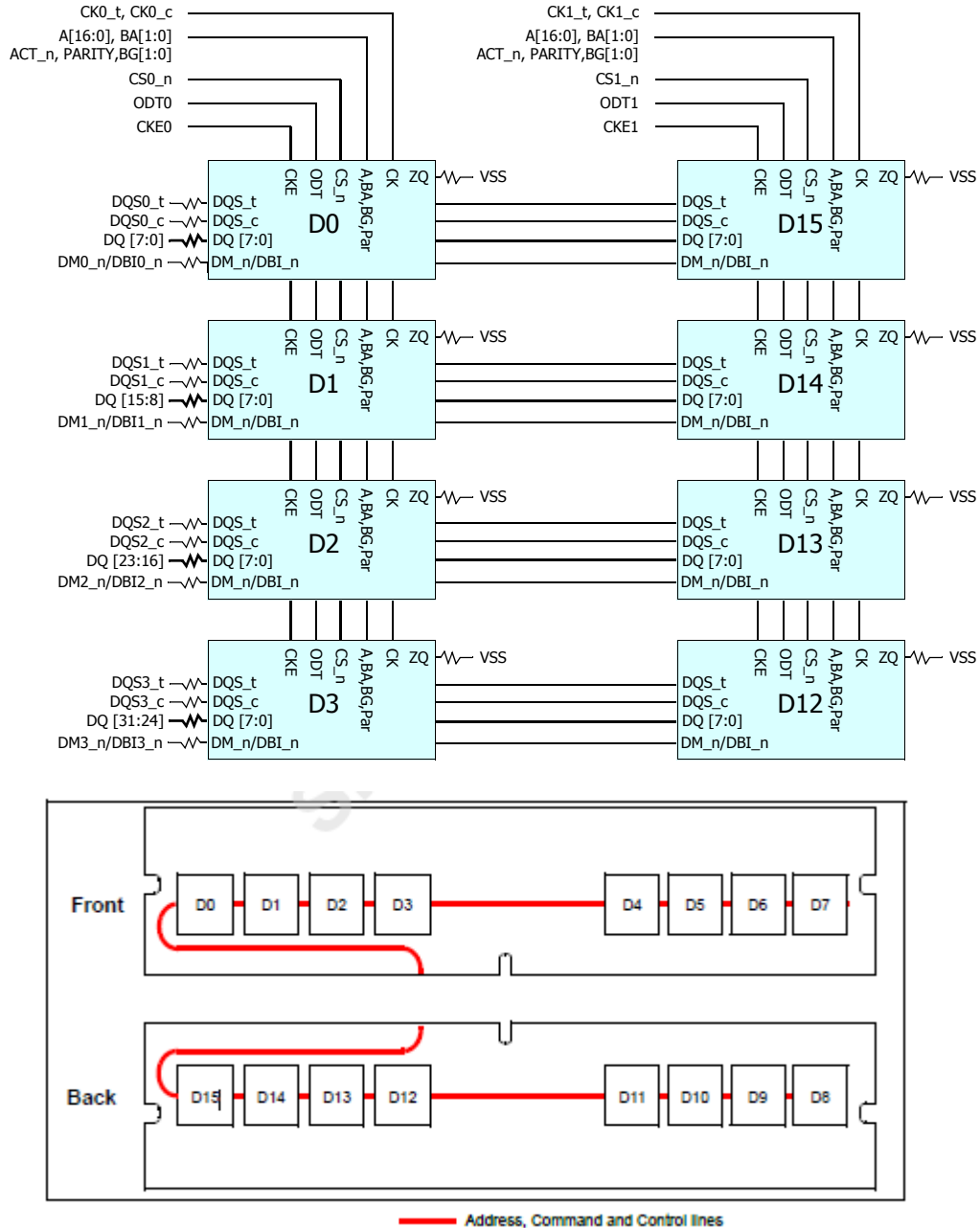
16GB, 2Gx64 Module(1Rank of x8) - page2



Note:

1. CK1_t, CK1_c terminated with $75 \Omega \pm 5\%$ resistor.
2. Unless otherwise noted, resistor values are $15 \Omega \pm 5\%$.
3. ZQ resistors are $240 \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.
4. EVENT_n isn't used for SPD without TS. Option Resistor for it should be unplaced.

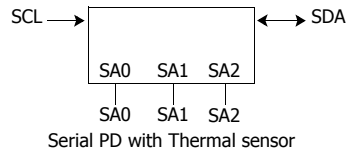
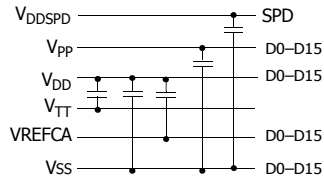
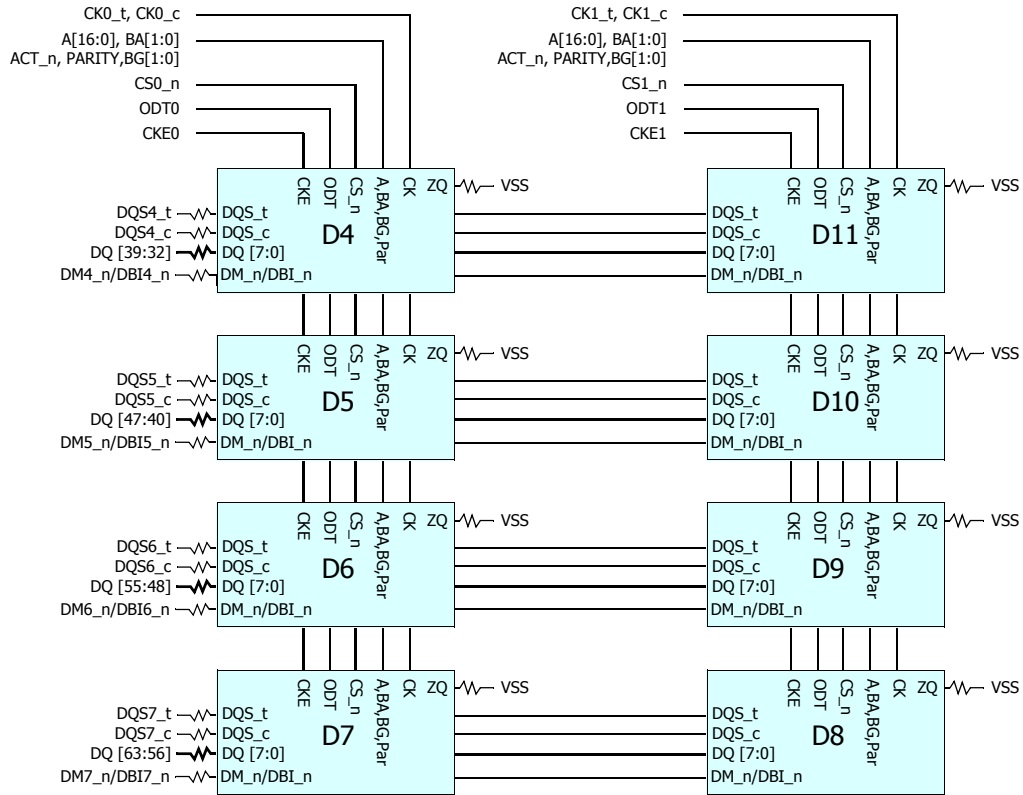
32GB, 4Gx64 Module(2Rank of x8) - page1



Note:

1. Unless otherwise noted, resistor values are $15\Omega \pm 5\%$.
2. ZQ resistors are $240\Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

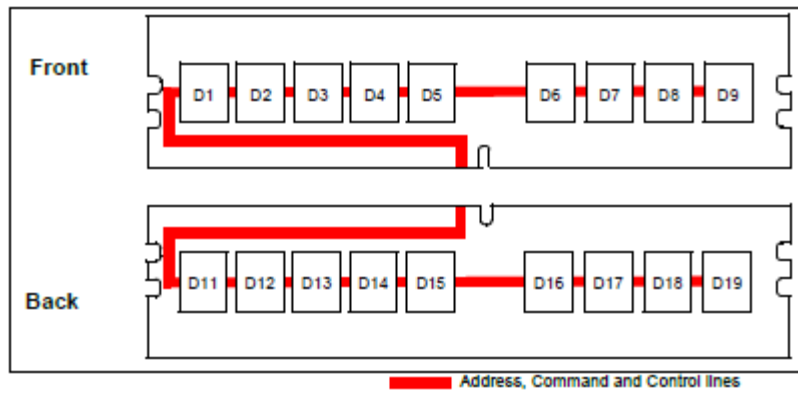
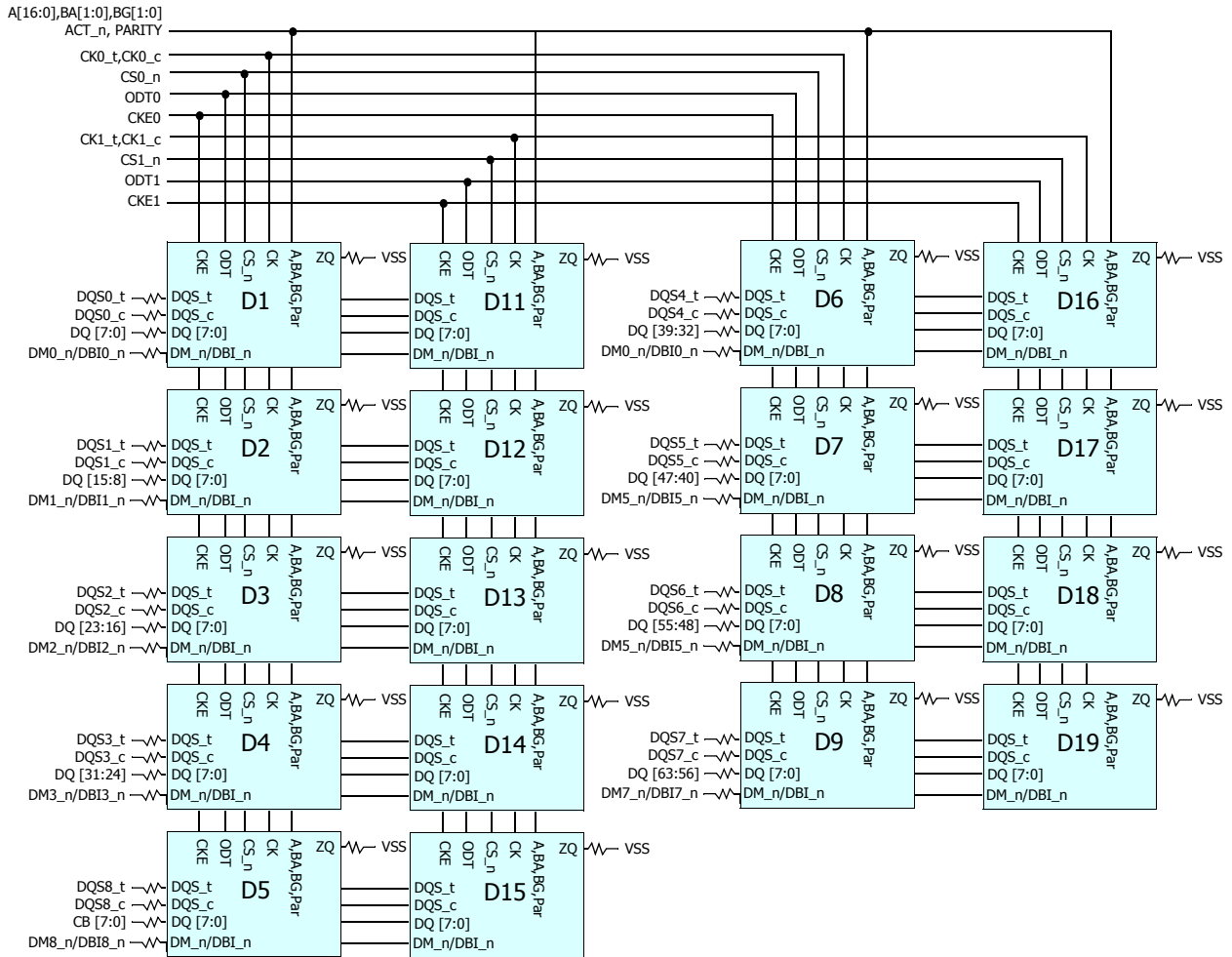
32GB, 4Gx64 Module(2Rank of x8) - page2



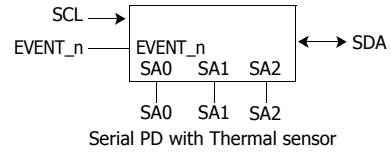
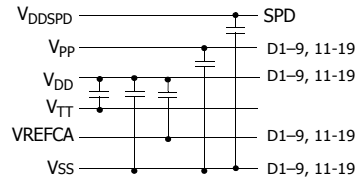
Note:

1. Unless otherwise noted, resistor values are $15\Omega \pm 5\%$.
2. ZQ resistors are $240\Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.
3. EVENT_n is not wired on this design.

32GB, 4Gx72 Module(2Rank of x8) - page1



32GB, 4Gx72 Module(2Rank of x8) - page2



Note:

1. Unless otherwise noted resistors are $15\ \Omega \pm 5\%$.
2. ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | NOTE |
|------------------------------------|--|-------------|-------|-------|
| VDD | Voltage on VDD pin relative to Vss | -0.3 ~ 1.5 | V | 1,3 |
| VDDQ | Voltage on VDDQ pin relative to Vss | -0.3 ~ 1.5 | V | 1,3 |
| VPP | Voltage on VPP pin relative to Vss | -0.3 ~ 3.0 | V | 4 |
| V _{IN} , V _{OUT} | Voltage on any pin except VREFCA relative to Vss | -0.3 ~ 1.5 | V | 1,3,5 |
| T _{STG} | Storage Temperature | -55 to +100 | °C | 1,2 |

NOTE :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
- VPP must be equal or greater than VDD/VDDQ at all times
- Overshoot area above 1.5V is specified in DDR4 Device Operation.

DRAM Component Operating Temperature Range

Temperature Range

| Symbol | Parameter | Rating | Units | Notes |
|-------------------|------------------------------------|----------|-------|-------|
| T _{OPER} | Normal Operating Temperature Range | 0 to 85 | °C | 1,2 |
| | Extended Temperature Range | 85 to 95 | °C | 1,3 |

Notes:

- Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

AC & DC Operating Conditions

Recommended DC Operating Conditions

Recommended DC Operating Conditions

| Symbol | Parameter | Rating | | | Unit | NOTE |
|--------|------------------------------------|--------|------|------|------|-------|
| | | Min. | Typ. | Max. | | |
| VDD | Supply Voltage | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| VDDQ | Supply Voltage for Output | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| VPP | Supply Voltage for DRAM Activating | 2.375 | 2.5 | 2.75 | V | 3 |

NOTE:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

AC & DC Input Measurement Levels

AC & DC Logic input levels for single-ended signals

Single-ended AC & DC input levels for Command and Address

| Symbol | Parameter | DDR4-1600/1866/2133/ 2400 | | DDR4-2666/3200 | | Unit | NOTE |
|--------------------|---------------------------------------|------------------------------|-----------------------|-----------------------|-----------------------|------|------|
| | | Min. | Max. | Min. | Max. | | |
| $V_{IH.CA}(DC75)$ | DC input logic high | $V_{REFCA}^+ - 0.075$ | VDD | $V_{REFCA}^+ - 0.065$ | VDD | V | |
| $V_{IL.CA}(DC75)$ | DC input logic low | VSS | $V_{REFCA}^- - 0.075$ | VSS | $V_{REFCA}^- - 0.065$ | V | |
| $V_{IH.CA}(AC100)$ | AC input logic high | $V_{REF} + 0.1$ | Note 2 | $V_{REF} + 0.09$ | Note 2 | V | 1 |
| $V_{IL.CA}(AC100)$ | AC input logic low | Note 2 | $V_{REF} - 0.1$ | Note 2 | $V_{REF} - 0.09$ | V | 1 |
| $V_{REFCA}(DC)$ | Reference Voltage for ADD, CMD inputs | $0.49 \cdot VDD$ | $0.51 \cdot VDD$ | $0.49 \cdot VDD$ | $0.51 \cdot VDD$ | V | 2,3 |

NOTE :

1. See "Overshoot and Undershoot Specifications"
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than $\pm 1\%$ VDD (for reference : approx. $\pm 12mV$)
3. For reference : approx. $VDD/2 \pm 12mV$

AC and DC Input Measurement Levels: V_{REF} Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure below. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA}).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than $\pm 1\% V_{DD}$.

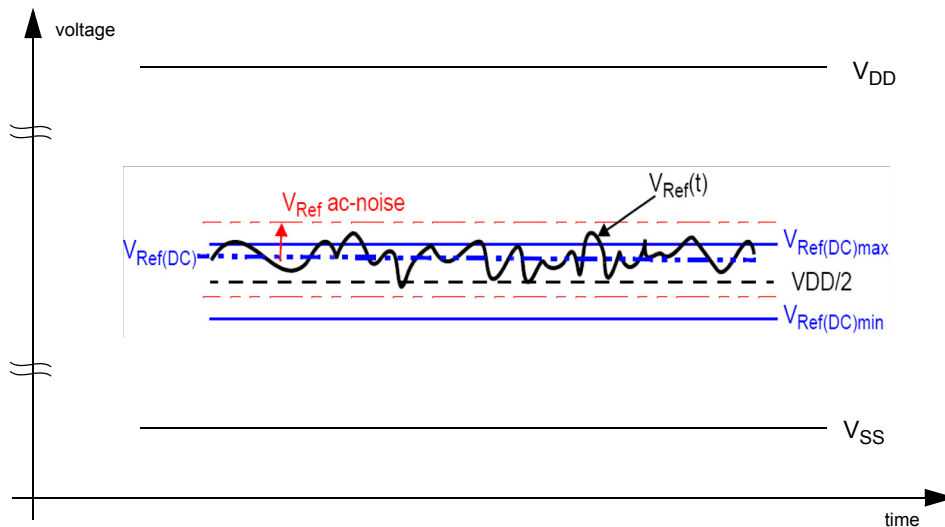


Illustration of $V_{REF}(DC)$ tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF} .

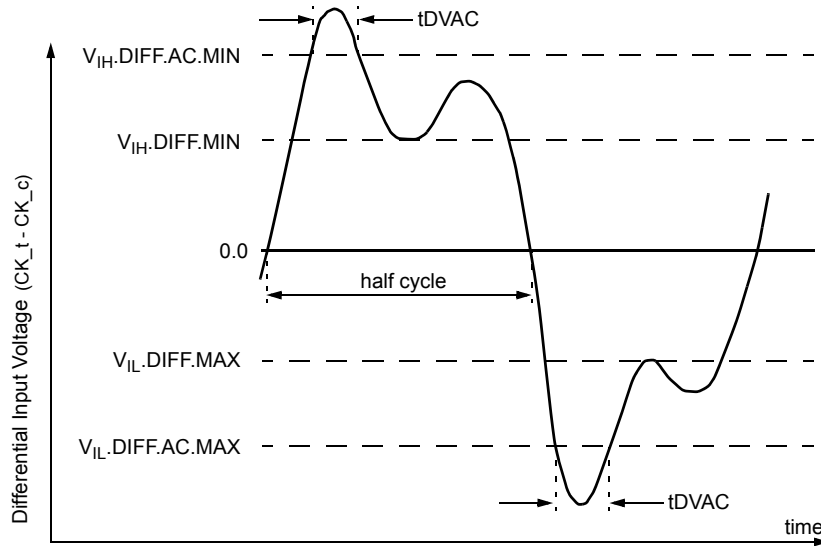
" V_{REF} " shall be understood as $V_{REF}(DC)$, as defined in Figure above.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit ($\pm 1\%$ of V_{DD}) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signal definition



NOTE:

1. Differential signal rising edge from $V_{IL.DIFF.MAX}$ to $V_{IH.DIFF.MIN}$ must be monotonic slope.
2. Differential signal falling edge from $V_{IH.DIFF.MIN}$ to $V_{IL.DIFF.MAX}$ must be monotonic slope.

Definition of differential ac-swing and "time above ac-level" t_{DVAC}

Differential swing requirements for clock (CK_t - CK_c) Differential AC and DC Input Levels

| Symbol | Parameter | DDR4 - 1600,1866,2133 | | DDR4 -2400 | | DDR4 -2666 | | DDR4 -2933 | | DDR4 -3200 | | unit | NOTE |
|---------------------|-------------------------|-----------------------|--------|------------|--------|------------|--------|------------|--------|------------|--------|------|------|
| | | min | max | min | max | min | max | min | max | min | max | | |
| V _{IHdiff} | differential input high | +0.150 | NOTE 3 | +0.135 | NOTE 3 | +0.135 | NOTE 3 | +0.125 | NOTE 3 | +0.110 | NOTE 3 | V | 1 |
| V _{ILdiff} | differential input low | NOTE 3 | -0.150 | NOTE 3 | -0.135 | NOTE 3 | -0.135 | NOTE 3 | -0.125 | NOTE 3 | -0.110 | V | 1 |

NOTE :

- Used to define a differential signal slew-rate.
- for CK_t - CK_c use V_{IH.CA}/V_{IL.CA}(AC) of ADD/CMD and V_{REFCA};
- These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits (V_{IH.CA}(DC) max, V_{IL.CA}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Allowed time before ringback (tDVAC) for CK_t - CK_c

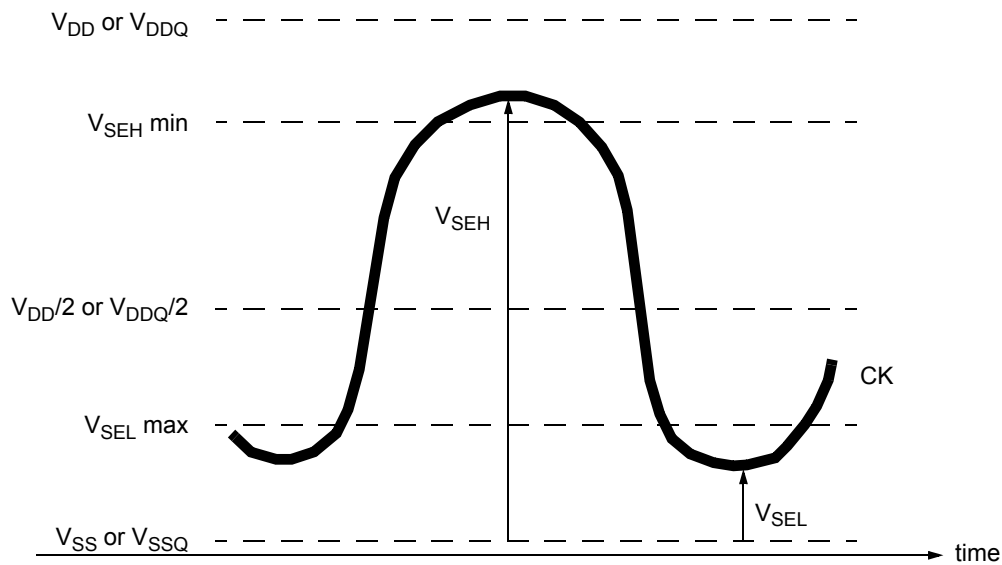
| Slew Rate [V/ns] | tDVAC [ps] @ V _{IH/Ldiff} (AC) = 200mV | | tDVAC [ps] @ V _{IH/Ldiff} (AC) = TBDmV | |
|------------------|---|-----|---|-----|
| | min | max | min | max |
| > 4.0 | 120 | - | TBD | - |
| 4.0 | 115 | - | TBD | - |
| 3.0 | 110 | - | TBD | - |
| 2.0 | 105 | - | TBD | - |
| 1.8 | 100 | - | TBD | - |
| 1.6 | 95 | - | TBD | - |
| 1.4 | 90 | - | TBD | - |
| 1.2 | 85 | - | TBD | - |
| 1.0 | 80 | - | TBD | - |
| < 1.0 | 80 | - | TBD | - |

Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach V_{SEH}min / V_{SEL}max (approximately equal to the ac-levels (V_{IH.CA(AC)} / V_{IL.CA(AC)}) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than V_{IH.CA(AC100)}/V_{IL.CA(AC100)} is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c



Single-ended requirement for differential signals

Note that, while ADD/CMD signal requirements are with respect to V_{refCA}, the single-ended components of differential signals have a requirement with respect to V_{DD} / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SEL}max, V_{SEH}min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK_t, CK_c

| Symbol | Parameter | DDR4-1600/ 1866/2133 | | DDR4-2400 | | DDR4-2666 | | DDR4-2933 | | DDR4-3200 | | Unit | NOTE |
|------------------|--|-------------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| V _{SEH} | Single-ended high-level for CK_t, CK_c | (VDD/2)+0.100 | NOTE3 | (VDD/2)+0.095 | NOTE3 | (VDD/2)+0.095 | NOTE3 | (VDD/2)+0.085 | NOTE3 | (VDD/2)+0.085 | NOTE3 | V | 1, 2 |
| V _{SEL} | Single-ended low-level for CK_t, CK_c | NOTE3 | (VDD/2)-0.100 | NOTE3 | (VDD/2)-0.095 | NOTE3 | (VDD/2)-0.095 | NOTE3 | (VDD/2)-0.085 | NOTE3 | (VDD/2)-0.085 | V | 1, 2 |

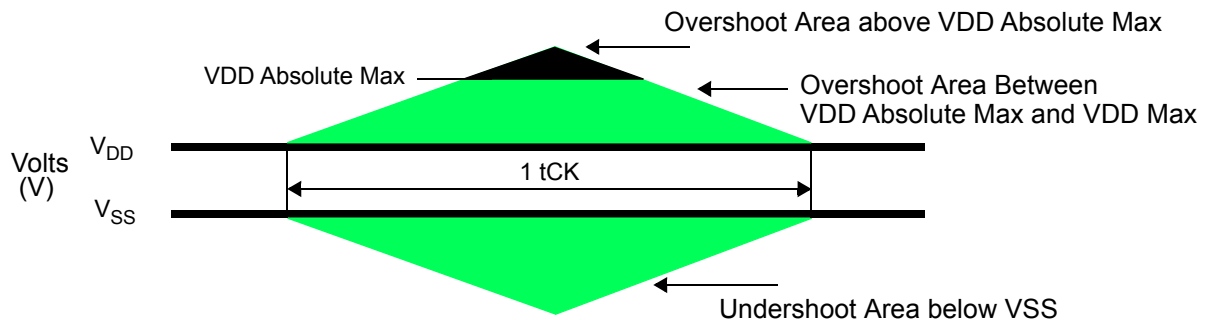
NOTE :

1. For CK_t - CK_c use V_{IH,CA}/V_{IL,CA}(AC) of ADD/CMD;
2. V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};
3. These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits (V_{IH,CA}(DC) max, V_{IL,CA}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Address and Control Overshoot and Undershoot specifications

AC overshoot/undershoot specification for Address, Command and Control pins

| Parameter | Specification | | | | | | | Unit |
|--|---------------|-----------|-----------|-----------|------------|-----------|-----------|------|
| | DDR4-1600 | DDR4-1866 | DDR4-2133 | DDR4-2400 | DDR4-2666 | DDR4-2933 | DDR4-3200 | |
| Maximum peak amplitude above VDD Absolute Max allowed for overshoot area | 0.06 | | | | 0.06 | | | V |
| Delta value between VDD Absolute Max and VDD Max allowed for overshoot area | VDD + 0.24 | | | | VDD + 0.24 | | | V |
| Maximum peak amplitude allowed for undershoot area | 0.30 | | | | 0.30 | | | V-ns |
| Maximum overshoot area per 1tCK Above Absolute Max | 0.0083 | 0.0071 | 0.0062 | 0.0055 | 0.0055 | | | V-ns |
| Maximum overshoot area per 1tCK Between Absolute Max | 0.2550 | 0.2185 | 0.1914 | 0.1699 | 0.1699 | | | V-ns |
| Maximum undershoot area per 1tCK Below VSS | 0.2644 | 0.2265 | 0.1984 | 0.1762 | 0.1762 | | | V-ns |
| (A0-A13,A17,BG0-BG1,BA0-BA1,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT,C2-C0) | | | | | | | | |

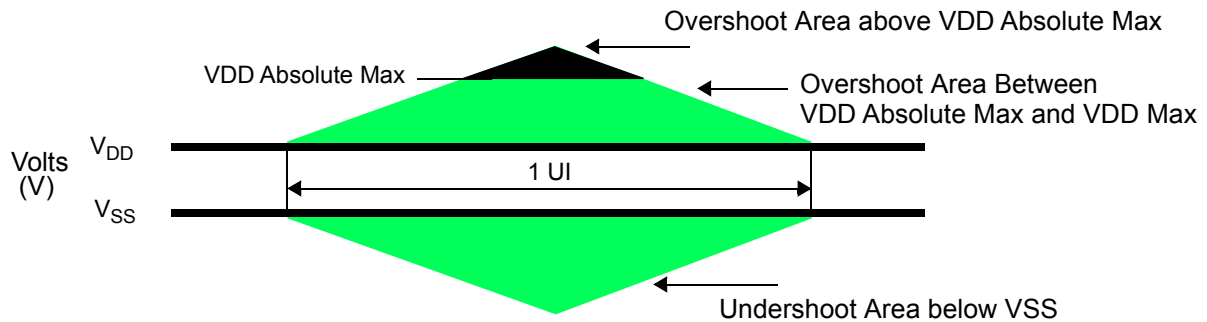


Address,Command and Control Overshoot and Undershoot Definition

Clock Overshoot and Undershoot Specifications

AC overshoot/undershoot specification for Clock

| Parameter | Specification | | | | | | | Unit |
|---|---------------|-----------|-----------|-----------|------------|-----------|-----------|------|
| | DDR4-1600 | DDR4-1866 | DDR4-2133 | DDR4-2400 | DDR4-2666 | DDR4-2933 | DDR4-3200 | |
| Maximum peak amplitude above VDD Absolute Max allowed for overshoot area | 0.06 | | | | 0.06 | | | V |
| Delta value between VDD Absolute Max and VDD Max allowed for overshoot area | VDD + 0.24 | | | | VDD + 0.24 | | | V |
| Maximum peak amplitude allowed for undershoot area | 0.30 | | | | 0.30 | | | V |
| Maximum overshoot area per 1UI Above Absolute Max | 0.0038 | 0.0032 | 0.0028 | 0.0025 | 0.0025 | | V-ns | |
| Maximum overshoot area per 1UI Between Absolute Max | 0.1125 | 0.0964 | 0.0844 | 0.0750 | 0.0750 | | V-ns | |
| Maximum undershoot area per 1UI Below VSS | 0.1144 | 0.0980 | 0.0858 | 0.0762 | 0.0762 | | V-ns | |
| (CK_t, Ck_c) | | | | | | | | |



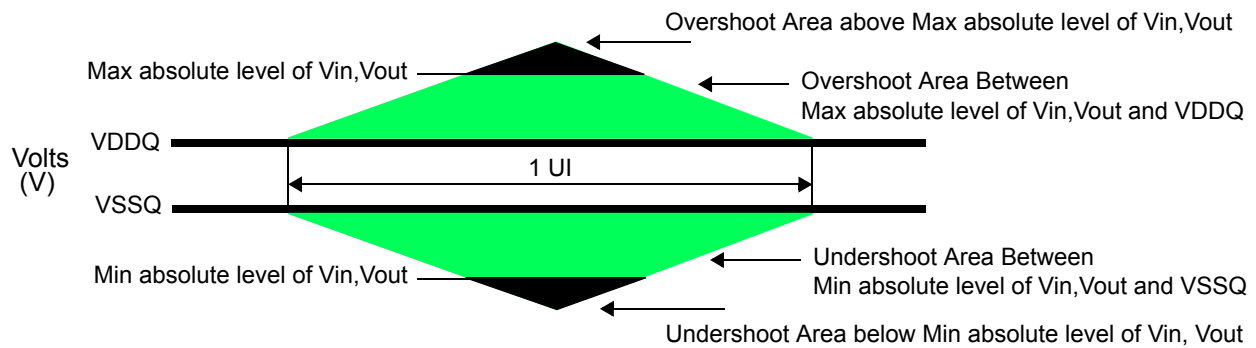
Clock Overshoot and Undershoot Definition

Data, Strobe and Mask Overshoot and Undershoot Specifications

AC overshoot/undershoot specification for Data, Strobe and Mask

| Parameter | Specification | | | | | | | Unit |
|--|---------------|-----------|-----------|-----------|-----------|-----------|-----------|------|
| | DDR4-1600 | DDR4-1866 | DDR4-2133 | DDR4-2400 | DDR4-2666 | DDR4-2933 | DDR4-3200 | |
| Maximum peak amplitude above Max absolute level of Vin,Vout | 0.16 | 0.16 | 0.16 | 0.16 | 0.16 | | | V |
| Overshoot area Between Max Absolute level of Vin, Vout and VDDQ Max | VDDQ + 0.24 | | | | VDDQ+0.24 | | | V |
| Undershoot area Between Min absolute level of Vin,Vout and VDDQ Max | 0.30 | 0.30 | 0.30 | 0.30 | 0.30 | | | V |
| Maximum peak amplitude below Min absolute level of Vin,Vout | 0.10 | 0.10 | 0.10 | 0.10 | 0.10 | | | V |
| Maximum overshoot area per 1UI Above Max absolute level of Vin,Vout | 0.0150 | 0.0129 | 0.0113 | 0.0100 | 0.0100 | | | V-ns |
| Maximum overshoot area per 1UI Between Max absolute level of Vin,Vout and VDDQ Max | 0.1050 | 0.0900 | 0.0788 | 0.0700 | 0.0700 | | | V-ns |
| Maximum undershoot area per 1UI Between Min absolute level of Vin,Vout and VSSQ | 0.1050 | 0.0900 | 0.0788 | 0.0700 | 0.0700 | | | V-ns |
| Maximum undershoot area per 1UI Below Min absolute level of Vin,Vout | 0.0150 | 0.0129 | 0.0113 | 0.0100 | 0.0100 | | | V-ns |

(DQ, DQS_t, DQS_c, DM_n, DBI_n, TDQS_t, TDQS_c)



Data, Strobe and Mask Overshoot and Undershoot Definition

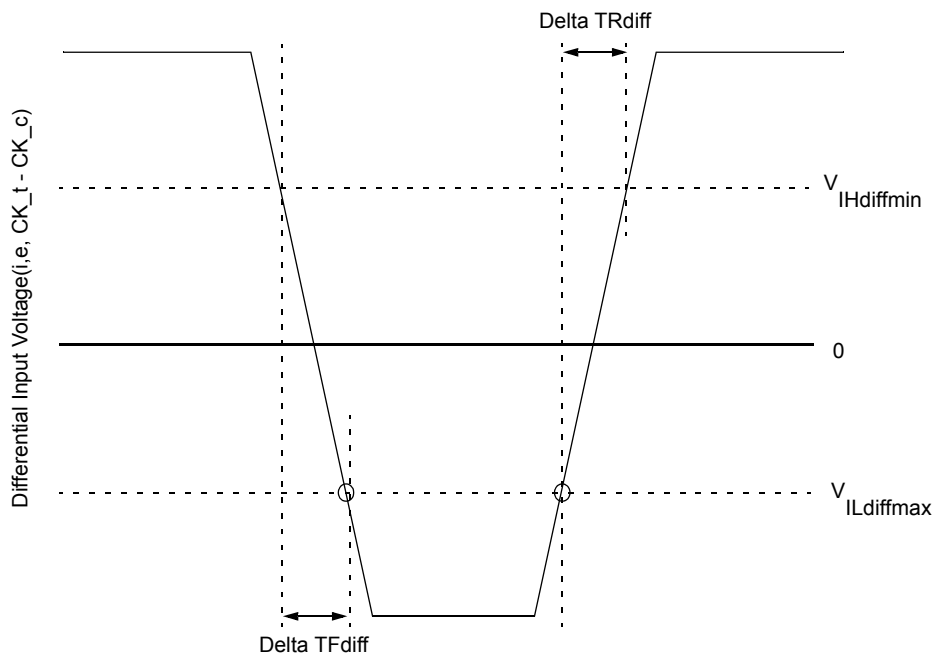
Slew Rate Definitions

Slew Rate Definitions for Differential Input Signals (CK)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Table and Figure below.

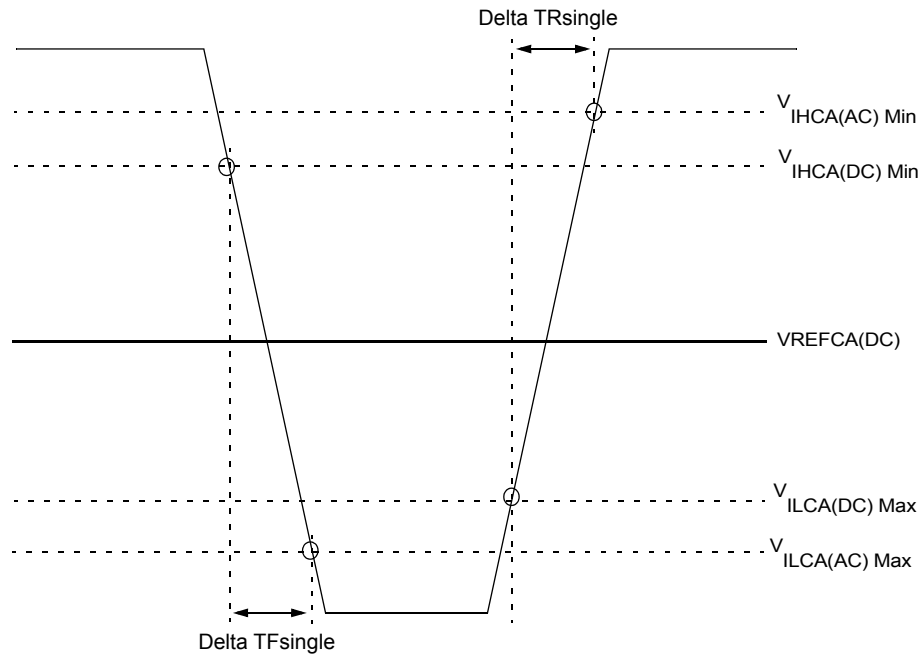
Differential Input Slew Rate Definition

| Description | | | Defined by |
|--|------------------------|------------------------|--|
| | from | to | |
| Differential input slew rate for rising edge(CK _t - CK _c) | V _{ILdiffmax} | V _{IHdiffmin} | $[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TR_{diff}$ |
| Differential input slew rate for falling edge(CK _t - CK _c) | V _{IHdiffmin} | V _{ILdiffmax} | $[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TF_{diff}$ |
| NOTE: The differential signal (i.e.,CK _t - CK _c) must be linear between these thresholds. | | | |



Differential Input Slew Rate Definition for CK_t, CK_c

Slew Rate Definition for Single-ended Input Signals (CMD/ADD)



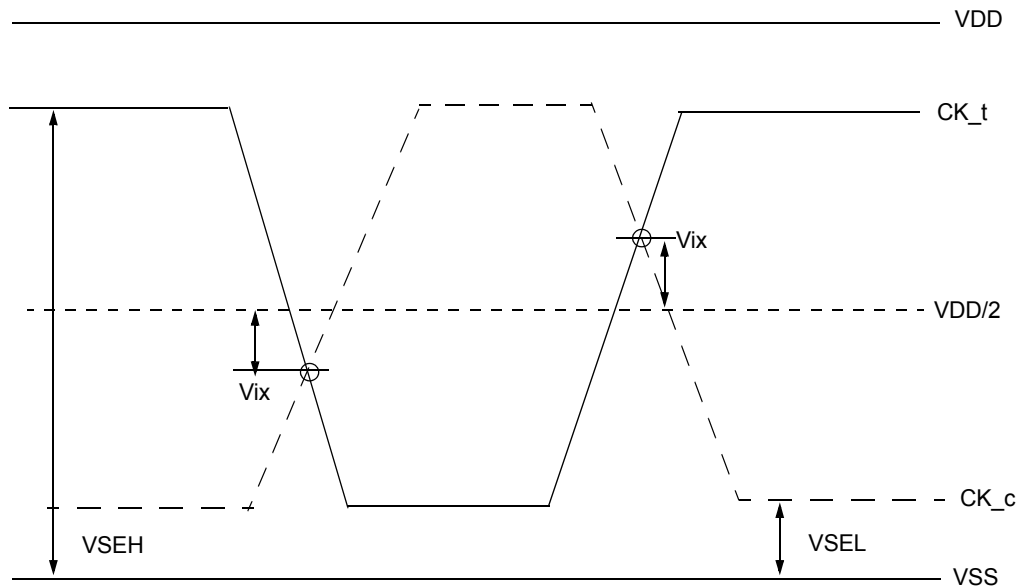
Single-ended Input Slew Rate definition for CMD and ADD

NOTE :

1. Single-ended input slew rate for rising edge = $\{ V_{IHCA(AC)Min} - V_{ILCA(DC)Max} \} / \Delta T_{Rsingle}$
2. Single-ended input slew rate for falling edge = $\{ V_{IHCA(DC)Min} - V_{ILCA(AC)Max} \} / \Delta T_{Fsingle}$
3. Single-ended signal rising edge from $V_{ILCA(DC)Max}$ to $V_{IHCA(DC)Min}$ must be monotonic slope.
4. Single-ended signal falling edge from $V_{IHCA(DC)Min}$ to $V_{ILCA(DC)Max}$ must be monotonic slope

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.



Vix Definition (CK)

Cross point voltage for differential input signals (CK)

| Symbol | Parameter | DDR4-1600/1866/2133 | | | |
|---------|---|---------------------------|--|--|---------------------------|
| | | min | | max | |
| - | Area of VSEH, VSEL | $VSEL \leq VDD/2 - 145mV$ | $VDD/2 - 145mV \leq VSEL \leq VDD/2 - 100mV$ | $VDD/2 + 100mV \leq VSEL \leq VDD/2 + 145mV$ | $VDD/2 + 145mV \leq VSEL$ |
| VIX(CK) | Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c | -120mV | $-(VDD/2 - VSEL) + 25mV$ | $(VSEH - VDD/2) - 25mV$ | 120mV |

| Symbol | Parameter | DDR4-2400/2666/3200 | | | |
|---------|---|---------------------------|--|--|---------------------------|
| | | min | | max | |
| - | Area of VSEH, VSEL | $VSEL \leq VDD/2 - 145mV$ | $VDD/2 - 145mV \leq VSEL \leq VDD/2 - 100mV$ | $VDD/2 + 100mV \leq VSEH \leq VDD/2 + 145mV$ | $VDD/2 + 145mV \leq VSEH$ |
| VIX(CK) | Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c | -120mV | $-(VDD/2 - VSEL) + 25mV$ | $(VSEH - VDD/2) - 25mV$ | 120mV |

CMOS rail to rail Input Levels

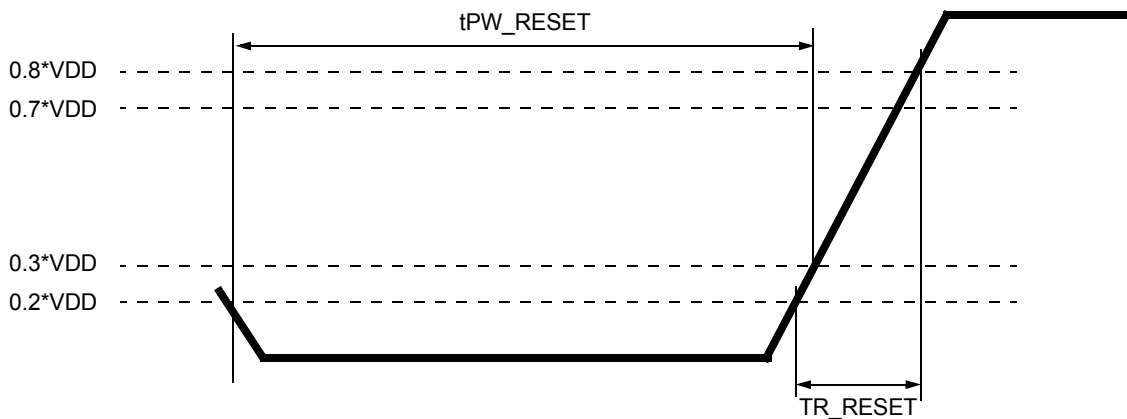
CMOS rail to rail Input Levels for RESET_n

CMOS rail to rail Input Levels for RESET_n

| Parameter | Symbol | Min | Max | Unit | NOTE |
|-----------------------|---------------|---------|---------|------|------|
| AC Input High Voltage | VIH(AC)_RESET | 0.8*VDD | VDD | V | 6 |
| DC Input High Voltage | VIH(DC)_RESET | 0.7*VDD | VDD | V | 2 |
| DC Input Low Voltage | VIL(DC)_RESET | VSS | 0.3*VDD | V | 1 |
| AC Input Low Voltage | VIL(AC)_RESET | VSS | 0.2*VDD | V | 7 |
| Rising time | TR_RESET | - | 1.0 | us | 4 |
| RESET pulse width | tPW_RESET | 1.0 | - | us | 3,5 |

NOTE :

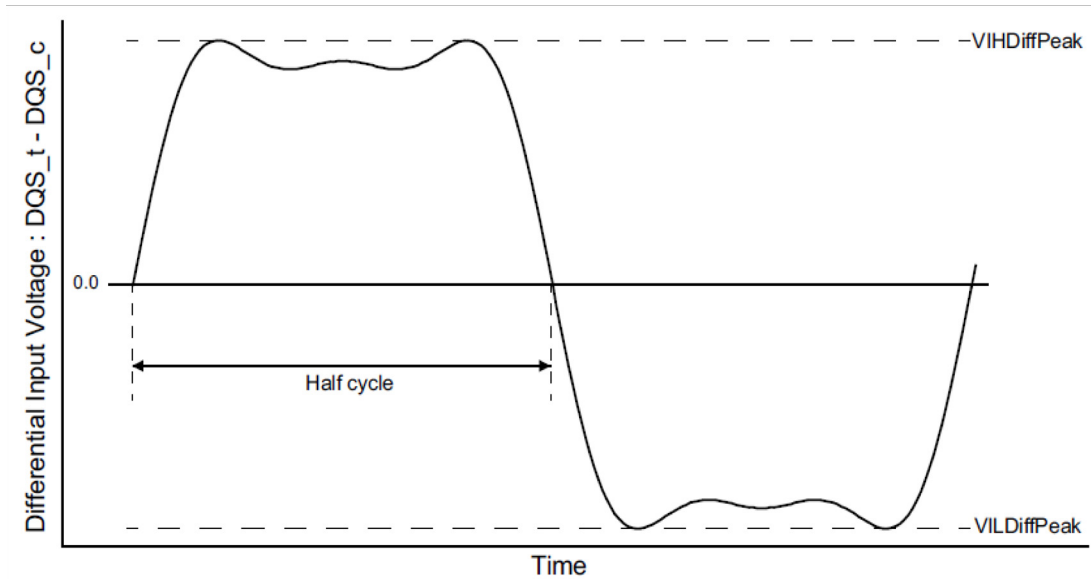
1. After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. No slope reversal(ringback) requirement during its level transition from Low to High.
5. This definition is applied only "Reset Procedure at Power Stable".
6. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings



RESET_n Input Slew Rate Definition

AC and DC Logic Input Levels for DQS Signals

Differential signal definition



Definition of differential DQS Signal AC-swing Level

Differential swing requirements for DQS (DQS_t - DQS_c)

Differential AC and DC Input Levels for DQS

| Symbol | Parameter | DDR4-1600,1866,2133 | | DDR4-2400 | | DDR4-2666,3200 | | Unit | Note |
|-------------|-----------------------|---------------------|-------|-----------|-------|----------------|-------|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| VIHDiffPeak | VIH.DIFF.Peak Voltage | 186 | Note2 | 160 | Note2 | 140 | Note2 | mV | 1 |
| VILDiffPeak | VIL.DIFF.Peak Voltage | Note2 | -186 | Note2 | -160 | Note2 | -140 | mV | 1 |

NOTE :

1. Used to define a differential signal slew-rate.
2. These values are not defined; however, the differential signals DQS_t - DQS_c, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

Peak voltage calculation method

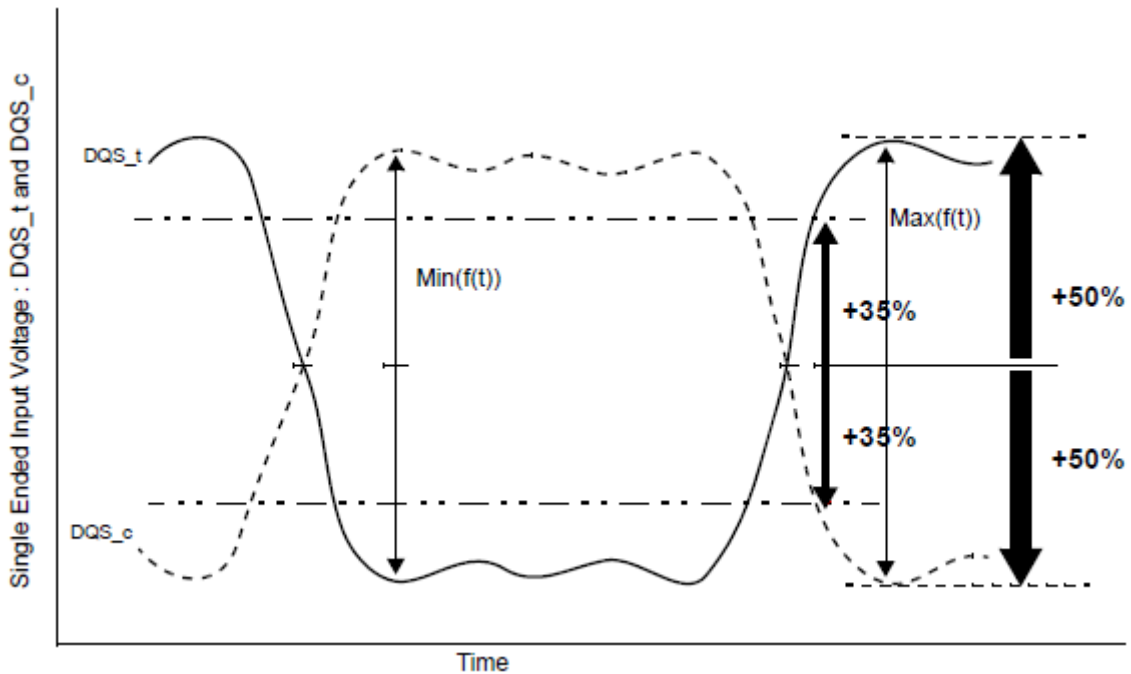
The peak voltage of Differential DQS signals are calculated in a following equation.

$$\mathbf{VIH.DIFF.Peak\ Voltage = Max(f(t))}$$

$$\mathbf{VIL.DIFF.Peak\ Voltage = Min(f(t))}$$

$$\mathbf{f(t) = VDQS_t - VDQS_c}$$

The Max(f(t)) or Min(f(t)) used to determine the midpoint which to reference the +/-35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all ui's.



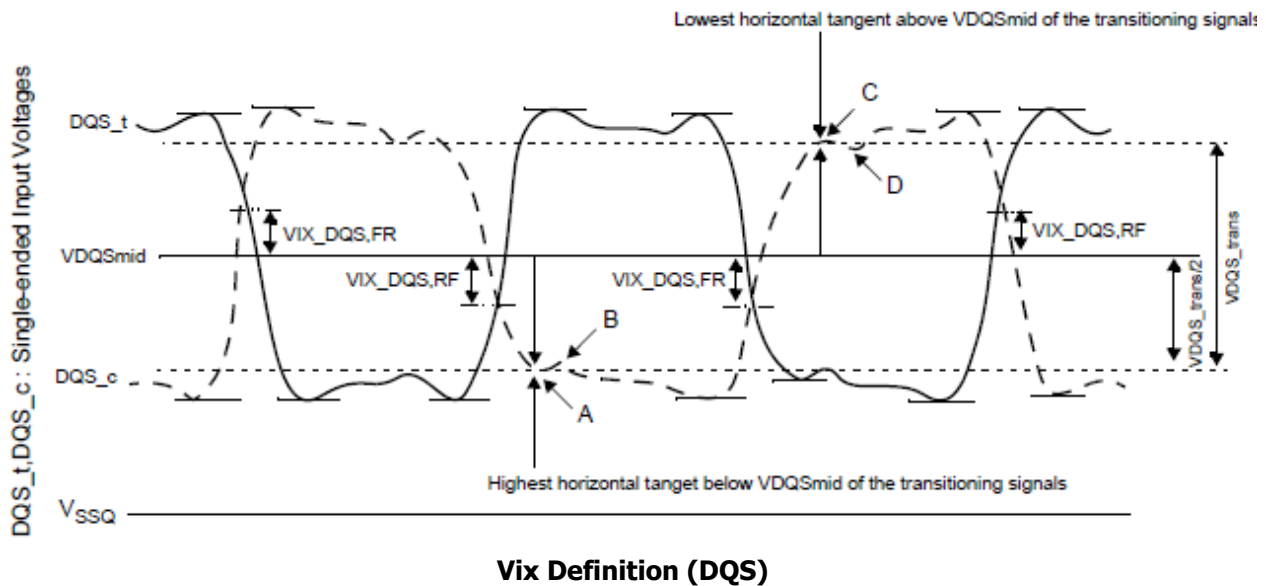
Definition of differential DQS Peak Voltage and range of exempt non-monotonic signaling

Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table below. The differential input cross point voltage VIX_{DQS} (VIX_{DQS_FR} and VIX_{DQS_RF}) is measured from the actual cross point of DQS_t, DQS_c relative to the VDQSmid for the DQS_t and DQS_c signals.

VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by VDQSmid. VDQSmid is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.

A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/- 30% of the midpoint of either VID.DIFF.Peak Voltage (DQS_t rising) or VIL.DIFF.Peak Voltage (DQS_c rising), refer to Future Definition of differential DQS Peak Voltage and range of exempt non-monotonic signaling. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Figure below) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Figure below) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Figure below) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Figure below) is not a valid horizontal tangent.



Cross point voltage for differential input signals

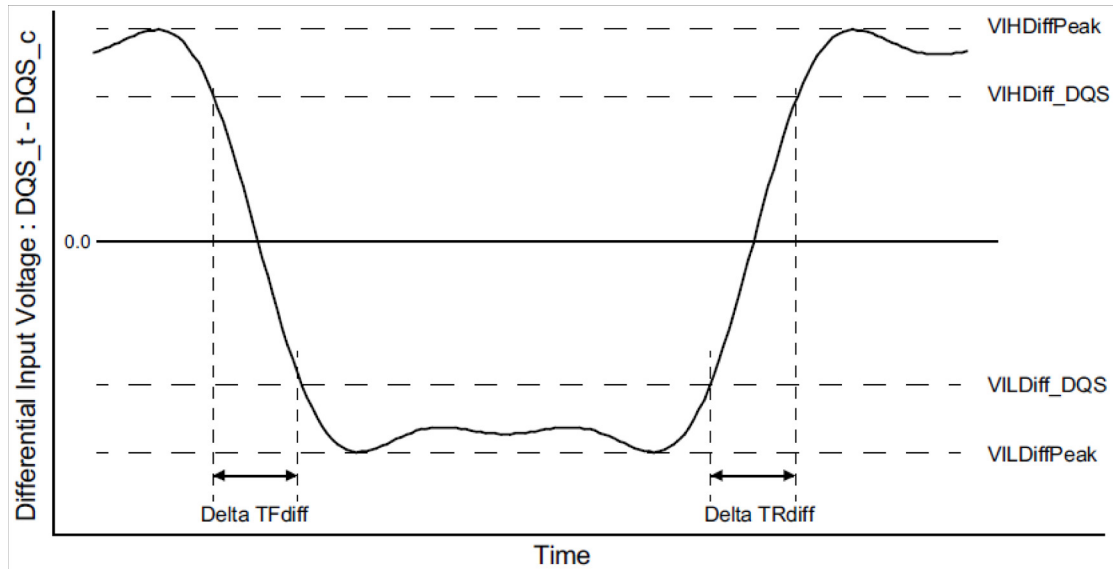
| Symbol | Parameter | DDR4-1600/1866/ 2133/2400 | | DDR4-2666/2933/ 3200 | | Unit | Note |
|----------------------|--|------------------------------|-------------------|-------------------------|-------------------|------|-------|
| | | Min | Max | Min | Max | | |
| Vix_DOS_ ratio | DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings | - | 25 | - | 25 | % | 1,2 |
| VDQSmid_to_ Vcent | VDQSmid offset relative to Vcent_DQ(midpoint) | - | min(VIH-diff, 50) | - | min(VIH-diff, 50) | mV | 3,4,5 |

NOTE :

1. Vix_DQS_Ratio is DQS VIX crossing (Vix_DQS_FR or Vix_DQS_RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
2. VDQSmid will be similar to the VREFDQ internal setting value obtained during Vref Training if the DQS and DQS drivers and paths are matched.
3. The maximum limit shall not exceed the smaller of VIHdiff minimum limit or 50mV.
4. VIX measurements are only applicable for transitioning DQS_t and DQS_c signals when toggling data, preamble and high-z states are not applicable conditions.
5. The parameter VDQSmid is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure below.



NOTE :

1. Differential signal rising edge from VILDiff_DQS to VIHDiff_DQS must be monotonic slope.
2. Differential signal falling edge from VIHDiff_DQS to VILDiff_DQS must be monotonic slope.

Differential Input Slew Rate Definition for DQS_t, DQS_c

Differential Input Slew Rate Definition for DQS_t, DQS_c

| Description | | | Defined by |
|---|-------------|-------------|---|
| | From | To | |
| Differential input slew rate for rising edge(DQS _t - DQS _c) | VILDiff_DQS | VIHDiff_DQS | $ VILDiff_DQS - VIHDiff_DQS / \Delta TRdiff$ |
| Differential input slew rate for falling edge(DQS _t - DQS _c) | VIHDiff_DQS | VILDiff_DQS | $ VILDiff_DQS - VIHDiff_DQS / \Delta TFdiff$ |

Differential Input Level for DQS_t, DQS_c

| Symbol | Parameter | DDR4-1600,1866,2133 | | DDR4-2400 | | DDR4-2666 | | DDR4-2933 | | DDR4-3200 | | Unit | Note |
|--------------|-------------------------|---------------------|------|-----------|------|-----------|------|-----------|------|-----------|------|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| VIHDif-f_DQS | Differential Input High | 136 | - | 130 | - | 130 | - | 115 | - | 110 | - | mV | |
| VILDif-f_DQS | Differential Input Low | - | -136 | - | -130 | - | -130 | - | -115 | - | -110 | mV | |

Differential Input Slew Rate for DQS_t, DQS_c

| Symbol | Parameter | DDR4-1600,1866,2133 | | DDR4-2400 | | DDR4-2666 | | DDR4-2933 | | DDR4-3200 | | Unit | Note |
|---------|------------------------------|---------------------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| SRIdiff | Differential Input Slew Rate | 3 | 18 | 3 | 18 | 2.5 | 18 | 2.5 | 18 | 2.5 | 18 | V/ns | |

AC and DC output Measurement levels

Single-ended AC & DC Output Levels

Single-ended AC & DC output levels

| Symbol | Parameter | DDR4-1600/1866/2133/ 2400/2666/3200 | Units | NOTE |
|----------------------|---|--|-------|------|
| V _{OH} (DC) | DC output high measurement level (for IV curve linearity) | 1.1 × V _{DDQ} | V | |
| V _{OM} (DC) | DC output mid measurement level (for IV curve linearity) | 0.8 × V _{DDQ} | V | |
| V _{OL} (DC) | DC output low measurement level (for IV curve linearity) | 0.5 × V _{DDQ} | V | |
| V _{OH} (AC) | AC output high measurement level (for output SR) | (0.7 + 0.15) × V _{DDQ} | V | 1 |
| V _{OL} (AC) | AC output low measurement level (for output SR) | (0.7 - 0.15) × V _{DDQ} | V | 1 |

NOTE :

1. The swing of $\pm 0.15 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $RZQ/7\Omega$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

Differential AC & DC Output Levels

Differential AC & DC output levels

| Symbol | Parameter | DDR4-1600/1866/ 2133/2400/2666/3200 | Units | NOTE |
|--------------------------|---|--|-------|------|
| V _{OHdiff} (AC) | AC differential output high measurement level (for output SR) | +0.3 × V _{DDQ} | V | 1 |
| V _{OLdiff} (AC) | AC differential output low measurement level (for output SR) | -0.3 × V _{DDQ} | V | 1 |

NOTE :

1. The swing of $\pm 0.3 \times V_{DDQ}$ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of $RZQ/7\Omega$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$ at each of the differential outputs.

Single-ended Output Slew Rate

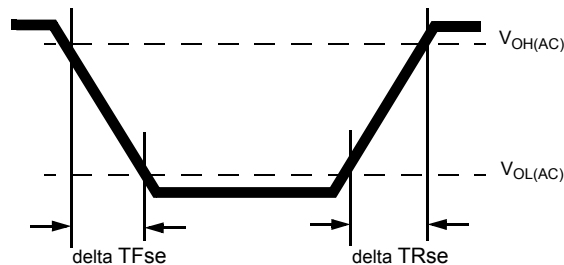
With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table and Figure below.

Single-ended output slew rate definition

| Description | Measured | | Defined by |
|--|--------------|--------------|--|
| | From | To | |
| Single ended output slew rate for rising edge | $V_{OL(AC)}$ | $V_{OH(AC)}$ | $[V_{OH(AC)} - V_{OL(AC)}] / \Delta TR_{se}$ |
| Single ended output slew rate for falling edge | $V_{OH(AC)}$ | $V_{OL(AC)}$ | $[V_{OH(AC)} - V_{OL(AC)}] / \Delta TF_{se}$ |

NOTE :

1. Output slew rate is verified by design and characterization, and may not be subject to production test.



Single-ended Output Slew Rate Definition

Single-ended output slew rate

| Parameter | Symbol | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | DDR4-2666 | | DDR4-2933 | | DDR4-3200 | | Units |
|-------------------------------|-------------------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Single ended output slew rate | SRQ _{se} | 4 | 9 | 4 | 9 | 4 | 9 | 4 | 9 | 4 | 9 | 4 | 9 | 4 | 9 | V/ns |

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

NOTE:

1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.

-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

Differential Output Slew Rate

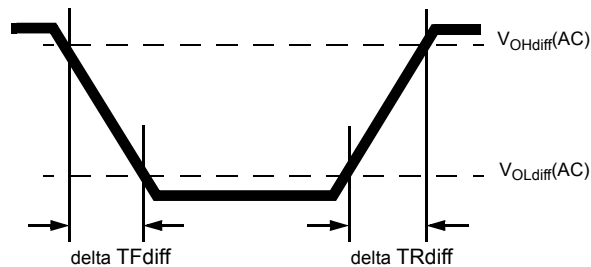
With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff}(AC)$ and $V_{OHdiff}(AC)$ for differential signals as shown in Table and Figure below.

Differential output slew rate definition

| Description | Measured | | Defined by |
|--|------------------|------------------|--|
| | From | To | |
| Differential output slew rate for rising edge | $V_{OLdiff}(AC)$ | $V_{OHdiff}(AC)$ | $[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / \Delta TR_{diff}$ |
| Differential output slew rate for falling edge | $V_{OHdiff}(AC)$ | $V_{OLdiff}(AC)$ | $[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / \Delta TF_{diff}$ |

NOTE :

- Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output Slew Rate Definition

Differential output slew rate

| Parameter | Symbol | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | DDR4-2666 | | DDR4-2933 | | DDR4-3200 | | Units |
|-------------------------------|---------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|----|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| Differential output slew rate | SRQdiff | 8 | 18 | 8 | 18 | 8 | 18 | 8 | 18 | 8 | 18 | 8 | 18 | 8 | 18 | V/ns |

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

For Ron = RZQ/7 setting

Single-ended AC & DC Output Levels of Connectivity Test Mode

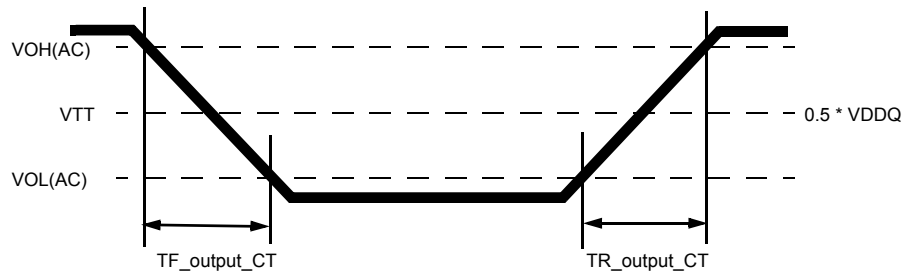
Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

Single-ended AC & DC output levels of Connectivity Test Mode

| Symbol | Parameter | DDR4-1600/1866/2133/ 2400/2666/3200 | Unit | Note |
|--------------|--|--|------|------|
| $V_{OH(DC)}$ | DC output high measurement level (for IV curve linearity) | $1.1 \times V_{DDQ}$ | V | |
| $V_{OM(DC)}$ | DC output mid measurement level (for IV curve linearity) | $0.8 \times V_{DDQ}$ | V | |
| $V_{OL(DC)}$ | DC output low measurement level (for IV curve linearity) | $0.5 \times V_{DDQ}$ | V | |
| $V_{OB(DC)}$ | DC output below measurement level (for IV curve linearity) | $0.2 \times V_{DDQ}$ | V | |
| $V_{OH(AC)}$ | AC output high measurement level (for output SR) | $V_{TT} + (0.1 \times V_{DDQ})$ | V | 1 |
| $V_{OL(AC)}$ | AC output below measurement level (for output SR) | $V_{TT} - (0.1 \times V_{DDQ})$ | V | 1 |

NOTE :

1. The effective test load is 50Ω terminated by $V_{TT} = 0.5 \times V_{DDQ}$.



Differential Output Slew Rate Definition of Connectivity Test Mode

Single-ended output slew rate of Connectivity Test Mode

| Parameter | Symbol | DDR4-1600/1866/2133/2400/2666/3200 | | Unit | Note |
|----------------------------|-------------------|------------------------------------|-----|------|------|
| | | Min | Max | | |
| Output signal Falling time | TF_{output_CT} | - | 10 | ns/V | |
| Output signal Rising time | TR_{output_CT} | - | 10 | ns/V | |

Standard Speed Bins

DDR4-1600 Speed Bins and Operations

| Speed Bin | | | DDR4-1600K | | Unit | NOTE | |
|---|---------|----------------------------|--|-----------------|------|------|-------------------|
| CL-nRCD-nRP | | | 11-11-11 | | | | |
| Parameter | Symbol | | min | max | | | |
| Internal read command to first data | tAA | | 13.75 ¹⁴ (13.50) ^{5,12} | 18.00 | ns | 12 | |
| Internal read command to first data with read DBI enabled | tAA_DBI | | tAA(min) + 2nCK | tAA(max) + 2nCK | ns | 12 | |
| ACT to internal read or write delay time | tRCD | | 13.75 (13.50) ^{5,12} | - | ns | 12 | |
| PRE command period | tRP | | 13.75 (13.50) ^{5,12} | - | ns | 12 | |
| ACT to PRE command period | tRAS | | 35 | 9 x tREFI | ns | 12 | |
| ACT to ACT or REF command period | tRC | | 48.75 (48.50) ^{5,12} | - | ns | 12 | |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 (Optional) 5 | tCK(AVG) | 1.5 | 1.6 | ns | 1,2,3,4, 11,14 |
| | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 1,2,3,4, 11 |
| CWL = 9,11 | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 11 | CL = 13 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,4 |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3 |
| Supported CL Settings | | | | (9),11,12 | | nCK | 13,14 |
| Supported CL Settings with read DBI | | | | (11),13,14 | | nCK | 13 |
| Supported CWL Settings | | | | 9,11 | | nCK | |

DDR4-1866 Speed Bins and Operations

| Speed Bin | | | DDR4-1866M | | Unit | NOTE | |
|---|---------|------------------------------------|--|-----------------|-------|-------|-------------------|
| CL-nRCD-nRP | | | 13-13-13 | | | | |
| Parameter | Symbol | | min | max | | | |
| Internal read command to first data | tAA | | 13.92 ¹⁴ (13.50) ^{5,12} | 18.00 | ns | 12 | |
| Internal read command to first data with read DBI enabled | tAA_DBI | | tAA(min) + 2nCK | tAA(max) + 2nCK | ns | 12 | |
| ACT to internal read or write delay time | tRCD | | 13.92 (13.50) ^{5,12} | - | ns | 12 | |
| PRE command period | tRP | | 13.92 (13.50) ^{5,12} | - | ns | 12 | |
| ACT to PRE command period | tRAS | | 34 | 9 x tREFI | ns | 12 | |
| ACT to ACT or REF command period | tRC | | 47.92 (47.50) ^{5,12} | - | ns | 12 | |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 (Optional) ⁵ | tCK(AVG) | 1.5 | 1.6 | ns | 1,2,3,4, 11,14 |
| | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 1,2,3,4, 11 |
| CWL = 9,11 | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 11 | CL = 13 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,4, 6 |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,6 |
| CWL = 10,12 | CL = 12 | CL = 14 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 13 | CL = 15 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,4 |
| | CL = 14 | CL = 16 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3 |
| Supported CL Settings | | | 9,11,12,13,14 | | nCK | 13,14 | |
| Supported CL Settings with read DBI | | | 11,13,14 15,16 | | nCK | 13 | |
| Supported CWL Settings | | | 9,10,11,12 | | nCK | | |

DDR4-2133 Speed Bins and Operations

| Speed Bin | | | DDR4-2133P | | Unit | NOTE |
|---|---------|----------|--|-----------------|--------|-------------------------|
| CL-nRCD-nRP | | | 15-15-15 | | | |
| Parameter | Symbol | | min | max | | |
| Internal read command to first data | tAA | | 14.06 ¹⁴ (13.50) ^{5,12} | 18.00 | ns | 12 |
| Internal read command to first data with read DBI enabled | tAA_DBI | | tAA(min) + 3nCK | tAA(max) + 3nCK | ns | 12 |
| ACT to internal read or write delay time | tRCD | | 14.06 (13.50) ^{5,12} | - | ns | 12 |
| PRE command period | tRP | | 14.06 (13.50) ^{5,12} | - | ns | 12 |
| ACT to PRE command period | tRAS | | 33 | 9 x tREFI | ns | 12 |
| ACT to ACT or REF command period | tRC | | 47.06 (46.50) ^{5,12} | - | ns | 12 |
| | Normal | Read DBI | | | | |
| CWL = 9 | CL = 9 | CL = 11 | tCK(AVG) | 1.5 | 1.6 | ns 1,2,3,4, 11,14 |
| | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns 1,2,3,11 |
| CWL = 9,11 | CL = 11 | CL = 13 | tCK(AVG) | 1.25 | <1.5 | ns 1,2,3,4, 7 |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns 1,2,3,7 |
| CWL = 10,12 | CL = 13 | CL = 15 | tCK(AVG) | 1.071 | <1.25 | ns 1,2,3,4, 7 |
| | CL = 14 | CL = 16 | tCK(AVG) | 1.071 | <1.25 | ns 1,2,3,7 |
| CWL = 11,14 | CL = 14 | CL = 17 | tCK(AVG) | Reserved | | ns 1,2,3,4 |
| | CL = 15 | CL = 18 | tCK(AVG) | 0.937 | <1.071 | ns 1,2,3,4 |
| | CL = 16 | CL = 19 | tCK(AVG) | 0.937 | <1.071 | ns 1,2,3 |
| Supported CL Settings | | | (9),(11),12,(13),14,15,16 | | nCK | 13,14 |
| Supported CL Settings with read DBI | | | (11),(13),14,(15),16,18,19 | | nCK | |
| Supported CWL Settings | | | 9,10,11,12,14 | | ns | 12 |

DDR4-2400 Speed Bins and Operations

| Speed Bin | | | DDR4-2400T | | Unit | NOTE | |
|---|---------|------------------------------------|----------------------------------|-----------------|--------|------|------------|
| CL-nRCD-nRP | | | 17-17-17 | | | | |
| Parameter | Symbol | | min | max | | | |
| Internal read command to first data | tAA | | 14.16 (13.75) ^{5,12} | 18.00 | ns | 12 | |
| Internal read command to first data with read DBI enabled | tAA_DBI | | tAA(min) + 3nCK | tAA(max) + 3nCK | ns | 12 | |
| ACT to internal read or write delay time | tRCD | | 14.16 (13.75) ^{5,12} | - | ns | 12 | |
| PRE command period | tRP | | 14.16 (13.75) ^{5,12} | - | ns | 12 | |
| ACT to PRE command period | tRAS | | 32 | 9 x tREFI | ns | 12 | |
| ACT to ACT or REF command period | tRC | | 46.16 (45.75) ^{5,12} | - | ns | 12 | |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 (Optional) ⁵ | tCK(AVG) | Reserved | | ns | 1,2,3,4,11 |
| | CL = 10 | CL = 12 | | 1.5 | 1.6 | ns | 1,2,3,4,11 |
| CWL = 9,11 | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 11 | CL = 13 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,4,8 |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,8 |
| CWL = 10,12 | CL = 12 | CL = 14 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 13 | CL = 15 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,4,8 |
| | CL = 14 | CL = 16 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,8 |
| CWL = 11,14 | CL = 14 | CL = 17 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 15 | CL = 18 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,4,8 |
| | CL = 16 | CL = 19 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,8 |
| CWL = 12,16 | CL = 15 | CL = 18 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 16 | CL = 19 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 17 | CL = 20 | tCK(AVG) | 0.833 | <0.937 | | |
| | CL = 18 | CL = 21 | tCK(AVG) | 0.833 | <0.937 | ns | 1,2,3 |
| Supported CL Settings | | | 10,11,12,13,14,15,16,17,18 | | nCK | 13 | |
| Supported CL Settings with read DBI | | | 12,13,14,15,16,18,19,20,21 | | nCK | | |
| Supported CWL Settings | | | 9,10,11,12,14,16 | | nCK | | |

DDR4-2666 Speed Bins and Operations

| Speed Bin | | | DDR4-2666V | | Unit | NOTE | |
|---|---------|----------|--|-----------------|--------|------------|-----------|
| CL-nRCD-nRP | | | 19-19-19 | | | | |
| Parameter | Symbol | | min | max | | | |
| Internal read command to first data | tAA | | 14.25 ¹⁴ (13.75) ^{5,12} | 18.00 | ns | 12 | |
| Internal read command to first data with read DBI enabled | tAA_DBI | | tAA(min) + 3nCK | tAA(max) + 3nCK | ns | 12 | |
| ACT to internal read or write delay time | tRCD | | 14.25 (13.75) ^{5,12} | - | ns | 12 | |
| PRE command period | tRP | | 14.25 (13.75) ^{5,12} | - | ns | 12 | |
| ACT to PRE command period | tRAS | | 32 | 9 x tREFI | ns | 12 | |
| ACT to ACT or REF command period | tRC | | 46.25 (45.75) ^{5,12} | - | ns | 12 | |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 | tCK(AVG) | Reserved | ns | 1,2,3,4,11 | |
| | CL = 10 | CL = 12 | tCK(AVG) | 1.5 | 1.6 | ns | 1,2,3,11 |
| CWL = 9,11 | CL = 10 | CL = 12 | tCK(AVG) | Reserved | ns | 4 | |
| | CL = 11 | CL = 13 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,4,9 |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,9 |
| CWL = 10,12 | CL = 12 | CL = 14 | tCK(AVG) | Reserved | ns | 4 | |
| | CL = 13 | CL = 15 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,4,9 |
| | CL = 14 | CL = 16 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,9 |
| CWL = 11,14 | CL = 14 | CL = 17 | tCK(AVG) | Reserved | ns | 4 | |
| | CL = 15 | CL = 18 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,4,9 |
| | CL = 16 | CL = 19 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,9 |
| CWL = 12,16 | CL = 15 | CL = 18 | tCK(AVG) | Reserved | ns | 4 | |
| | CL = 16 | CL = 19 | tCK(AVG) | Reserved | ns | 1,2,3,4,9 | |
| | CL = 17 | CL = 20 | tCK(AVG) | 0.833 | <0.937 | ns | 1,2,3,4,9 |
| | CL = 18 | CL = 21 | tCK(AVG) | 0.833 | <0.937 | ns | 1,2,3 |
| CWL = 14,18 | CL = 17 | CL = 20 | tCK(AVG) | Reserved | ns | 1,2,3,4 | |
| | CL = 18 | CL = 21 | tCK(AVG) | Reserved | ns | 1,2,3,4 | |
| | CL = 19 | CL = 22 | tCK(AVG) | 0.75 | <0.833 | ns | 1,2,3,4 |
| | CL = 20 | CL = 23 | tCK(AVG) | 0.75 | <0.833 | ns | 1,2,3 |
| Supported CL Settings | | | 10,(11),12,(13),14,(15),16,(17),18,19,20 | | nCK | 13 | |
| Supported CL Settings with read DBI | | | 12,(13),14,(15),17,(18),19,(20),21,22,23 | | nCK | | |
| Supported CWL Settings | | | 9,10,11,12,14,16,18 | | nCK | | |

DDR4-2933 Speed Bins and Operations

| Speed Bin | | | DDR4-2933Y | | Unit | NOTE | |
|---|---------|----------|--|-----------------|--------|------|------------|
| CL-nRCD-nRP | | | 21-21-21 | | | | |
| Parameter | Symbol | | min | max | | | |
| Internal read command to first data | tAA | | 14.32 ¹⁴ (13.75) ^{5,12} | 18.00 | ns | 12 | |
| Internal read command to first data with read DBI enabled | tAA_DBI | | tAA(min) + 4nCK | tAA(max) + 4nCK | ns | 12 | |
| ACT to internal read or write delay time | tRCD | | 14.32 (13.75) ^{5,12} | - | ns | 12 | |
| PRE command period | tRP | | 14.32 (13.75) ^{5,12} | - | ns | 12 | |
| ACT to PRE command period | tRAS | | 32 | 9 x tREFI | ns | 12 | |
| ACT to ACT or REF command period | tRC | | 46.32 (45.75) ^{5,12} | - | ns | 12 | |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 | tCK(AVG) | Reserved | | ns | 1,2,3,4,11 |
| | CL = 10 | CL = 12 | tCK(AVG) | 1.5 | 1.6 | ns | 1,2,3,11 |
| CWL = 9,11 | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 11 | CL = 13 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,4,13 |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,15 |
| CWL = 10,12 | CL = 12 | CL = 14 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 13 | CL = 15 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,4,15 |
| | CL = 14 | CL = 16 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,15 |
| CWL = 11,14 | CL = 14 | CL = 17 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 15 | CL = 18 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,4,15 |
| | CL = 16 | CL = 19 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,15 |
| CWL = 12,16 | CL = 15 | CL = 18 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 16 | CL = 19 | tCK(AVG) | Reserved | | ns | 1,2,3,4,15 |
| | CL = 17 | CL = 20 | tCK(AVG) | 0.833 | 0.937 | ns | 1,2,3,4,15 |
| | CL = 18 | CL = 21 | tCK(AVG) | 0.833 | 0.937 | ns | 1,2,3,15 |
| CWL = 14,18 | CL = 17 | CL = 20 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 18 | CL = 21 | tCK(AVG) | Reserved | | ns | 1,2,3,4,15 |
| | CL = 19 | CL = 22 | tCK(AVG) | 0.75 | <0.833 | ns | 1,2,3,4,15 |
| | CL = 20 | CL = 23 | tCK(AVG) | 0.75 | <0.833 | ns | 1,2,3,15 |
| CWL = 16,20 | CL = 19 | CL = 23 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 20 | CL = 24 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 21 | CL = 26 | tCK(AVG) | 0.682 | <0.75 | ns | 1,2,3,4 |
| | CL = 22 | CL = 26 | tCK(AVG) | 0.682 | <0.75 | ns | 1,2,3 |
| Supported CL Settings | | | 10,(11),12,(13),14,(15),16,(17),18,(19),20,21,22 | | nCK | 13 | |
| Supported CL Settings with read DBI | | | 12,(13),14,(15),16,(18),19,(20),21,(22),23,25,26 | | nCK | 13 | |
| Supported CWL Settings | | | 9,10,11,12,14,15,16,18,20 | | nCK | | |

DDR4-3200 Speed Bins and Operations

| Speed Bin | | | DDR4-3200AA | | Unit | NOTE | |
|---|---------|----------|--|-----------------|--------|------------|------------|
| CL-nRCD-nRP | | | 22-22-22 | | | | |
| Parameter | Symbol | | min | max | | | |
| Internal read command to first data | tAA | | 13.75 | 18.00 | ns | 12 | |
| Internal read command to first data with read DBI enabled | tAA_DBI | | tAA(min) + 4nCK | tAA(max) + 4nCK | ns | 12 | |
| ACT to internal read or write delay time | tRCD | | 13.75 | - | ns | 12 | |
| PRE command period | tRP | | 13.75 | - | ns | 12 | |
| ACT to PRE command period | tRAS | | 32 | 9 x tREFI | ns | 12 | |
| ACT to ACT or REF command period | tRC | | 45.75 | - | ns | 12 | |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 | tCK(AVG) | Reserved | ns | 1,2,3,4,11 | |
| | CL = 10 | CL = 12 | tCK(AVG) | Reserved | ns | 1,2,3,4,11 | |
| CWL = 9,11 | CL = 10 | CL = 12 | tCK(AVG) | Reserved | ns | 1,2,3,4 | |
| | CL = 11 | CL = 13 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,4,10 |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,10 |
| CWL = 10,12 | CL = 12 | CL = 14 | tCK(AVG) | Reserved | ns | 1,2,3,4 | |
| | CL = 13 | CL = 15 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,4,10 |
| | CL = 14 | CL = 16 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,10 |
| CWL = 11,14 | CL = 14 | CL = 17 | tCK(AVG) | Reserved | ns | 1,2,3,4 | |
| | CL = 15 | CL = 18 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,4,10 |
| | CL = 16 | CL = 19 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,10 |
| CWL = 12,16 | CL = 15 | CL = 18 | tCK(AVG) | Reserved | ns | 1,2,3,4 | |
| | CL = 16 | CL = 19 | tCK(AVG) | Reserved | ns | 1,2,3,4,10 | |
| | CL = 17 | CL = 20 | tCK(AVG) | 0.833 | <0.937 | ns | 1,2,3,4,10 |
| | CL = 18 | CL = 21 | tCK(AVG) | 0.833 | <0.937 | ns | 1,2,3,10 |
| CWL = 14,18 | CL = 17 | CL = 20 | tCK(AVG) | Reserved | ns | 1,2,3,4 | |
| | CL = 18 | CL = 21 | tCK(AVG) | Reserved | ns | 1,2,3,4,10 | |
| | CL = 19 | CL = 22 | tCK(AVG) | 0.75 | <0.833 | ns | 1,2,3,4,10 |
| | CL = 20 | CL = 23 | tCK(AVG) | 0.75 | <0.833 | ns | 1,2,3,10 |
| CWL = 16,20 | CL = 20 | CL = 24 | tCK(AVG) | Reserved | ns | 1,2,3,4 | |
| | CL = 22 | CL = 26 | tCK(AVG) | 0.625 | <0.75 | ns | 1,2,3,4 |
| | CL = 24 | CL = 28 | tCK(AVG) | 0.625 | <0.75 | ns | 1,2,3 |
| Supported CL Settings | | | 10,11,12,13,14,15, 16,17,18,19,20,22, 24 | | nCK | 13 | |
| Supported CL Settings with read DBI | | | 12,13,14,15,16,18, 19,20,21,22,23,24, 26, 28 | | nCK | | |
| Supported CWL Settings | | | 9,10,11,12,14,16, 18,20 | | nCK | | |

Speed Bin Table Note

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133, 2400, 2933 and 3200 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section 13.5.
3. tCK(avg).MAX limits: Calculate $tCK(avg) = tAA.MAX / CL\ SELECTED$ and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
11. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12. DDR4-2400,2666,2933 and 3200Mbps speed bin support CL=10 if DRAM operate at 1333MT/s data rate.
13. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
14. CL number in parentheses, it means that these numbers are optional.
15. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
16. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

IDD and IDDQ Specification Parameters and Test Conditions

IDD, IPP and IDDQ Measurement Conditions

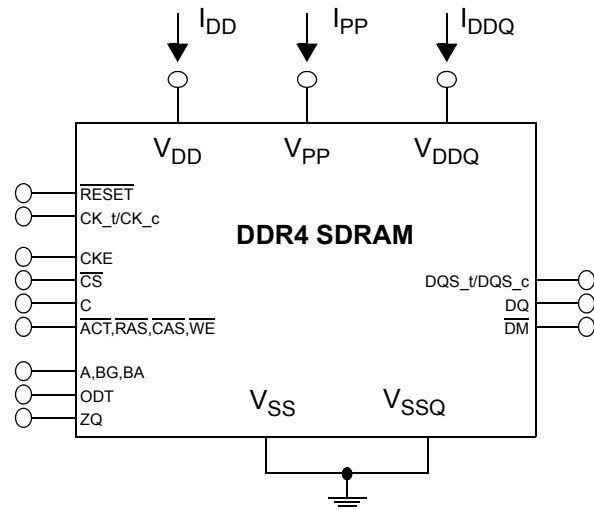
In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as $V_{IN} \leq V_{ILAC}(\max)$.
- "1" and "HIGH" is defined as $V_{IN} \geq V_{IHAC}(\min)$.
- "MID-LEVEL" is defined as inputs are $V_{REF} = V_{DD} / 2$.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 11.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
 - RON = RZQ/7 (34 Ohm in MR1);
 - RTT_NOM = RZQ/6 (40 Ohm in MR1);
 - RTT_WR = RZQ/2 (120 Ohm in MR2);
 - RTT_PARK = Disable;
 - Qoff = 0_B (Output Buffer enabled) in MR1;
 - TDQS_t disabled in MR1;
 - CRC disabled in MR2;
 - CA parity feature disabled in MR5;
 - Gear down mode disabled in MR3
 - Read/Write DBI disabled in MR5;
 - DM disabled in MR5
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define $D = \{CS_n, ACT_n, RAS_n, CAS_n, WE_n\} := \{HIGH, LOW, LOW, LOW, LOW\}$; apply BG/BA changes when directed.
- Define $D\# = \{CS_n, ACT_n, RAS_n, CAS_n, WE_n\} := \{HIGH, HIGH, HIGH, HIGH, HIGH\}$; apply invert of BG/BA changes when directed above.



NOTE:

1. DIMM level Output test load condition may be different from above

Figure 1 - Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

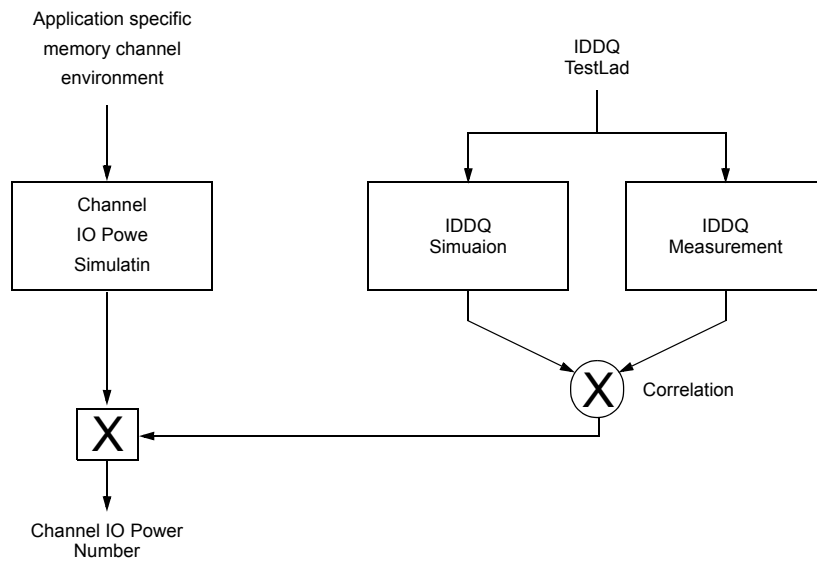


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1-Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

| Symbol | DDR4-1600 | DDR4-1866 | DDR4-2133 | DDR4-2400 | DDR4-2666 | DDR4-2933 | DDR4-3200 | Unit |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|------|
| | 11-11-11 | 13-13-13 | 15-15-15 | 17-17-17 | 19-19-19 | 21-21-21 | 22-22-22 | |
| tCK | 1.25 | 1.071 | 0.937 | 0.833 | 0.75 | 0.682 | 0.625 | ns |
| CL | 11 | 13 | 15 | 17 | 19 | 21 | 22 | nCK |
| CWL | 11 | 12 | 14 | 16 | 18 | 20 | 20 | nCK |
| nRCD | 11 | 13 | 15 | 17 | 19 | 21 | 22 | nCK |
| nRC | 39 | 45 | 51 | 56 | 62 | 68 | 74 | nCK |
| nRAS | 28 | 32 | 36 | 39 | 43 | 47 | 52 | nCK |
| nRP | 11 | 13 | 15 | 17 | 19 | 21 | 22 | nCK |
| nFAW | x4 | 16 | 16 | 16 | 16 | 16 | 16 | nCK |
| | x8 | 20 | 22 | 23 | 26 | 28 | 31 | nCK |
| | x16 | 28 | 28 | 32 | 36 | 40 | 44 | nCK |
| nRRDS | x4 | 4 | 4 | 4 | 4 | 4 | 4 | nCK |
| | x8 | 4 | 4 | 4 | 4 | 4 | 4 | nCK |
| | x16 | 5 | 5 | 6 | 7 | 8 | 8 | nCK |
| nRRDL | x4 | 5 | 5 | 6 | 6 | 7 | 8 | nCK |
| | x8 | 5 | 5 | 6 | 6 | 7 | 8 | nCK |
| | x16 | 6 | 6 | 7 | 8 | 9 | 10 | nCK |
| tCCD_S | 4 | 4 | 4 | 4 | 4 | 4 | 4 | nCK |
| tCCD_L | 5 | 5 | 6 | 6 | 7 | 8 | 8 | nCK |
| tWTR_S | 2 | 3 | 3 | 3 | 4 | 4 | 4 | nCK |
| tWTR_L | 6 | 7 | 8 | 9 | 10 | 11 | 12 | nCK |
| nRFC 2Gb | 128 | 150 | 171 | 193 | 214 | 235 | 256 | nCK |
| nRFC 4Gb | 208 | 243 | 278 | 313 | 347 | 382 | 416 | nCK |
| nRFC 8Gb | 280 | 327 | 374 | 421 | 467 | 514 | 560 | nCK |
| nRFC 16Gb | 280 | 327 | 374 | 421 | 467 | 514 | 560 | nCK |

Table 2 -Basic IDD, IPP and IDDQ Measurement Conditions

| Symbol | Description |
|--------------------|---|
| IDD0 | Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 3; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 3 |
| IDD0A | Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0 |
| IPP0 | Operating One Bank Active-Precharge IPP Current Same condition with IDD0 |
| IDD1 | Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling according to Table 4; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 4); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 4 |
| IDD1A | Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1 |
| IPP1 | Operating One Bank Active-Read-Precharge IPP Current Same condition with IDD1 |
| IDD2N | Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 5 |
| IDD2NA | Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N |
| IPP2N | Precharge Standby IPP Current Same condition with IDD2N |
| IDD2NT | Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 6; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: toggling according to Table 6; Pattern Details: see Table 6 |
| IDDQ2NT (Optional) | Precharge Standby ODT IDDQ Current Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current |
| IDD2NL | Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled ³ |
| IDD2NG | Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled ^{3,5} |
| IDD2ND | Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled ³ |

| | |
|-----------------------|--|
| IDD2N_par | Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled ³ |
| IDD2P | Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0 |
| IPP2P | Precharge Power-Down IPP Current Same condition with IDD2P |
| IDD2Q | Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0 |
| IDD3N | Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 5 |
| IDD3NA | Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N |
| IPP3N | Active Standby IPP Current Same condition with IDD3N |
| IDD3P | Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0 |
| IPP3P | Active Power-Down IPP Current Same condition with IDD3P |
| IDD4R | Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ² ; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 7); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 7 |
| IDD4RA | Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R |
| IDD4RB | Operating Burst Read Current with Read DBI Read DBI enabled³, Other conditions: see IDD4R |
| IPP4R | Operating Burst Read IPP Current Same condition with IDD4R |
| IDDQ4R (Optional) | Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current |
| IDDQ4RB (Optional) | Operating Burst Read IDDQ Current with Read DBI Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current |

| | |
|-----------|---|
| IDD4W | Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless write data burst with different data between one burst and the next one according to Table 8; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 8); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at HIGH; Pattern Details: see Table 8 |
| IDD4WA | Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W |
| IDD4WB | Operating Burst Write Current with Write DBI Write DBI enabled³, Other conditions: see IDD4W |
| IDD4WC | Operating Burst Write Current with Write CRC Write CRC enabled³, Other conditions: see IDD4W |
| IDD4W_par | Operating Burst Write Current with CA Parity CA Parity enabled³, Other conditions: see IDD4W |
| IPP4W | Operating Burst Write IPP Current Same condition with IDD4W |
| IDD5B | Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC (see Table 9); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 9 |
| IPP5B | Burst Refresh Write IPP Current (1X REF) Same condition with IDD5B |
| IDD5F2 | Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B |
| IPP5F2 | Burst Refresh Write IPP Current (2X REF) Same condition with IDD5F2 |
| IDD5F4 | Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B |
| IPP5F4 | Burst Refresh Write IPP Current (4X REF) Same condition with IDD5F4 |
| IDD6N | Self Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL |
| IPP6N | Self Refresh IPP Current: Normal Temperature Range Same condition with IDD6N |
| IDD6E | Self-Refresh Current: Extended Temperature Range⁵⁾ T_{CASE}: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL |
| IPP6E | Self Refresh IPP Current: Extended Temperature Range Same condition with IDD6E |

| | |
|-------|---|
| IDD6R | Self-Refresh Current: Reduced Temperature Range T_{CASE} for CT devices 0 to 45°C; Low Power Array Self Refresh (LP ASR) : Reduced ⁴ ; CKE : Low; External clock : Off; CK_t and CK_c#: LOW; CL : see Table 1; BL : 8 ¹ ; AL : 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO : High; DM_n :stable at 1; Bank Activity : Extended Temperature Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL |
| IPP6R | Self Refresh IPP Current: Reduced Temperature Range Same condition with IDD6R |
| IDD6A | Auto Self-Refresh Current T_{CASE} for CT devices 0 to 95°C; Low Power Array Self Refresh (LP ASR) : Auto ⁴ ; CKE : Low; External clock : Off; CK_t and CK_c#: LOW; CL : see Table 1; BL : 8 ¹ ; AL : 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO : High; DM_n :stable at 1; Bank Activity : Auto Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL |
| IPP6A | Auto Self-Refresh IPP Current Same condition with IDD6A |
| IDD7 | Operating Bank Interleave Read Current CKE : High; External clock : On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL : see Table 1; BL : 8 ¹ ; AL : CL-1; CS_n : High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs : partially toggling according to Table 10; Data IO : read data bursts with different data between one burst and the next one according to Table 10; DM_n : stable at 1; Bank Activity : two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 10; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : stable at 0; Pattern Details : see Table 10 |
| IPP7 | Operating Bank Interleave Read IPP Current Same condition with IDD7 |
| IDD8 | Maximum Power Down Current TBD |
| IPP8 | Maximum Power Down IPP Current Same condition with IDD8 |

NOTE :

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable
 - set MR1 [A12 = 0] : Qoff = Output buffer enabled
 - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
 - RTT_Nom enable
 - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6
 - RTT_WR enable
 - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2
 - RTT_PARK disable
 - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
010] : 1866MT/s, 2133MT/s
011] : 2400MT/s
 - Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate
 - DLL disabled : set MR1 [A0 = 0]
 - CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
010] : 2400MT/s
 - Read DBI enabled : set MR5 [A12 = 1]
 - Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
 - 01] : Reduced Temperature range
 - 10] : Extended Temperature range
 - 11] : Auto Self Refresh
5. IDD2NG should be measured after sync pulse(NOP) input.

Table 3 - IDD0, IDD0A and IPP0 Measurement-Loop Pattern¹

| CK_t / CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n/ A16 | CAS_n/ A15 | WE_n/ A14 | ODT | C[2:0] ³ | BG[1:0] ² | BA[1:0] | A12/BC_n | A[17,13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data ⁴ | | | |
|-------------|-------------|--|--------------|--|------|-------|------------|------------|-----------|-----|---------------------|----------------------|----------------|----------|-------------|----------|--------|--------|--------|-------------------|---|---|---|
| toggling | Static High | 0 | 0 | ACT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | |
| | | | 1,2 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | | 3,4 | D_#, D_# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 7 | F | 0 | 0 | - | |
| | | | ... | repeat pattern 1...4 until nRAS - 1, truncate if necessary | | | | | | | | | | | | | | | | | | | |
| | | | nRAS | PRE | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | ... | repeat pattern 1...4 until nRC - 1, truncate if necessary | | | | | | | | | | | | | | | | | | | |
| | | 1 | 1*nRC | repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | |
| | | 2 | 2*nRC | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | |
| | | 3 | 3*nRC | repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | |
| | | 4 | 4*nRC | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | |
| | | 5 | 5*nRC | repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | |
| | | 6 | 6*nRC | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | |
| | | 7 | 7*nRC | repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | |
| | | 8 | 8*nRC | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | |
| | | 9 | 9*nRC | repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | |
| 10 | 10*nRC | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | | | |
| 11 | 11*nRC | repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | | |
| 12 | 12*nRC | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | | | |
| 13 | 13*nRC | repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | | | |
| 14 | 14*nRC | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | | |
| 15 | 15*nRC | repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | | | |

NOTE:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

Table 4 - IDD1, IDD1A and IPP1 Measurement-Loop Pattern^{a)}

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n/A16 | CAS_n/A15 | WE_n/A14 | ODT | C[2:0] ³ | BG[1:0] ² | BA[1:0] | A12/BC_n | A[17,13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data ⁴ | | |
|------------|-------------|--|--------------|--|--------|-------|-----------|-----------|----------|-----|---------------------|----------------------|----------------|----------|-------------|----------|--------|--------|--------|-------------------|--|--|
| toggling | Static High | 0 | 0 | WR | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF | |
| | | | 1 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | | 2,3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 3 ² | 3 | 0 | 0 | 0 | 7 | F | 0 | - | |
| | | 1 | 4 | WR | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 7 | F | 0 | 0 | 0 | D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 |
| | | | | 5 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | | 6,7 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 3 ² | 3 | 0 | 0 | 0 | 7 | F | 0 | - | |
| | | 2 | 8-11 | repeat Sub-Loop 0, use BG[1:0] ² = 0, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 3 | 12-15 | repeat Sub-Loop 1, use BG[1:0] ² = 1, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | 4 | 16-19 | repeat Sub-Loop 0, use BG[1:0] ² = 0, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 5 | 20-23 | repeat Sub-Loop 1, use BG[1:0] ² = 1, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 6 | 24-27 | repeat Sub-Loop 0, use BG[1:0] ² = 0, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | 7 | 28-31 | repeat Sub-Loop 1, use BG[1:0] ² = 1, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | 8 | 32-35 | repeat Sub-Loop 0, use BG[1:0] ² = 2, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | 9 | 36-39 | repeat Sub-Loop 1, use BG[1:0] ² = 3, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 10 | 40-43 | repeat Sub-Loop 0, use BG[1:0] ² = 2, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| 11 | 44-47 | repeat Sub-Loop 1, use BG[1:0] ² = 3, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | |
| 12 | 48-51 | repeat Sub-Loop 0, use BG[1:0] ² = 2, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | | |
| 13 | 52-55 | repeat Sub-Loop 1, use BG[1:0] ² = 3, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | | |
| 14 | 56-59 | repeat Sub-Loop 0, use BG[1:0] ² = 2, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | |
| 15 | 60-63 | repeat Sub-Loop 1, use BG[1:0] ² = 3, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | | |

NOTE:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

Table 5 - IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P

Measurement-Loop Pattern¹

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n/A16 | CAS_n/A15 | WE_n/A14 | ODT | C[2:0] ³ | BG[1:0] ² | BA[1:0] | A12/BC_n | A[17,13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data ⁴ | | |
|------------|-------------|--|--------------|--|------|-------|-----------|-----------|----------|-----|---------------------|----------------------|----------------|----------|-------------|----------|--------|--------|--------|-------------------|---|---|
| toggling | Static High | 0 | 0 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | | 1 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | 2 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 0 | 7 | F | 0 | 0 |
| | | | 3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 0 | 7 | F | 0 | 0 |
| | | 1 | 4-7 | repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 2 | 8-11 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 3 | 12-15 | repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | 4 | 16-19 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 5 | 20-23 | repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 6 | 24-27 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | 7 | 28-31 | repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | 8 | 32-35 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | 9 | 36-39 | repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 10 | 40-43 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 11 | 44-47 | repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | 12 | 48-51 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| 13 | 52-55 | repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | | |
| 14 | 56-59 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | |
| 15 | 60-63 | repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | | |

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern¹

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n/A16 | CAS_n/A15 | WE_n/A14 | ODT | C[2:0] ³ | BG[1:0] ² | BA[1:0] | A12/BC_n | A[17,13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data ⁴ | | |
|------------|-------------|--|--------------|--|------|-------|-----------|-----------|----------|-----|---------------------|----------------------|----------------|----------|-------------|----------|--------|--------|--------|-------------------|---|---|
| toggling | Static High | 0 | 0 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | | 1 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | 2 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 7 | F | 0 | 0 | - |
| | | | 3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 7 | F | 0 | 0 | - |
| | | 1 | 4-7 | repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 1, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 2 | 8-11 | repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 0, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 3 | 12-15 | repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 1, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | 4 | 16-19 | repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 0, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 5 | 20-23 | repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 1, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 6 | 24-27 | repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 0, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | 7 | 28-31 | repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 1, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | 8 | 32-35 | repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 2, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | 9 | 36-39 | repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 3, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 10 | 40-43 | repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 2, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 11 | 44-47 | repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 3, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| 12 | 48-51 | repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 2, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | | |
| 13 | 52-55 | repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 3, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | | |
| 14 | 56-59 | repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 2, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | |
| 15 | 60-63 | repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 3, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | | |

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

Table 7 - IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern¹

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n/A16 | CAS_n/A15 | WE_n/A14 | ODT | C[2:0] ³ | BG[1:0] ² | BA[1:0] | A12/BC_n | A[17,13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data ⁴ | | | |
|------------|-------------|--|--------------|--|--------|-------|-----------|-----------|----------|-----|---------------------|----------------------|----------------|----------------|-------------|----------|--------|--------|--------|-------------------|--|--|---|
| toggling | Static High | 0 | 0 | RD | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF | | |
| | | | 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | | 2,3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 0 | 7 | F | 0 | - | |
| | | 1 | 4 | RD | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 7 | F | 0 | D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 | |
| | | | | 5 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | | 6,7 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 0 | 7 | F | 0 | - |
| | | 2 | 8-11 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | |
| | | 3 | 12-15 | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | |
| | | 4 | 16-19 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | |
| | | 5 | 20-23 | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | |
| | | 6 | 24-27 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | |
| | | 7 | 28-31 | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | |
| | | 8 | 32-35 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | |
| | | 9 | 36-39 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | |
| | | 10 | 40-43 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | |
| 11 | 44-47 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | | |
| 12 | 48-51 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | | | |
| 13 | 52-55 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | | | |
| 14 | 56-59 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | | |
| 15 | 60-63 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | | | |

NOTE :

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command.

Table 8 - IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern¹

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n/A16 | CAS_n/A15 | WE_n/A14 | ODT | C[2:0] ³ | BG[1:0] ² | BA[1:0] | A12/BC_n | A[17,13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data ⁴ | | |
|------------|-------------|--|--------------|--|--------|-------|-----------|-----------|----------|-----|---------------------|----------------------|----------------|----------------|-------------|----------|--------|--------|--------|-------------------|--|--|
| toggling | Static High | 0 | 0 | WR | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF | |
| | | | 1 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | | 2,3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 0 | 7 | F | 0 | - |
| | | 1 | 4 | WR | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 7 | F | 0 | D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 |
| | | | | 5 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | | 6,7 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 0 | 7 | F | 0 |
| | | 2 | 8-11 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 3 | 12-15 | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | 4 | 16-19 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 5 | 20-23 | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 6 | 24-27 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | 7 | 28-31 | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | 8 | 32-35 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | 9 | 36-39 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 10 | 40-43 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| 11 | 44-47 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | |
| 12 | 48-51 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | | |
| 13 | 52-55 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | | |
| 14 | 56-59 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | |
| 15 | 60-63 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | | |

NOTE :

1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command.

Table 9 - IDD4WC Measurement-Loop Pattern¹

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n/A16 | CAS_n/A15 | WE_n/A14 | ODT | C[2:0] ^c | BG[1:0] ^b | BA[1:0] | A12/BC_n | A[17,13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data ^d | | |
|------------|-------------|--|--------------|--|------|-------|-----------|-----------|----------|-----|---------------------|----------------------|---------|----------|-------------|----------|--------|--------|--------|-------------------|--|--|
| toggling | Static High | 0 | 0 | WR | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC | |
| | | 1,2 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | 3,4 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 3 ² | 3 | 0 | 0 | 0 | 0 | 7 | F | 0 | - | |
| | | 5 | WR | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 7 | F | 0 | 0 | D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC | |
| | | 6,7 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | 8,9 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 3 ² | 3 | 0 | 0 | 0 | 0 | 7 | F | 0 | - | |
| | | 2 | 10-14 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 3 | 15-19 | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | 4 | 20-24 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 5 | 25-29 | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | 6 | 30-34 | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | 7 | 35-39 | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | 8 | 40-44 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | 9 | 45-49 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | 10 | 50-54 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| 11 | 55-59 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | |
| 12 | 60-64 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | | |
| 13 | 65-69 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | | |
| 14 | 70-74 | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | | |
| 15 | 75-79 | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | | |

For x4 and x8 only

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Write Command.

Table 10 - IDD5B Measurement-Loop Pattern¹

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n/A16 | CAS_n/A15 | WE_n/A14 | ODT | C[2:0] ³ | BG[1:0] ² | BA[1:0] | A12/BC_n | A[17,13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data ⁴ | | |
|------------|-------------|----------|--------------|---|---|-------|-----------|-----------|----------|-----|---------------------|----------------------|----------------|----------|-------------|----------|--------|--------|--------|-------------------|---|---|
| toggling | Static High | 0 | 0 | REF | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | |
| | | 1 | 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | | 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | 3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 0 | 7 | F | 0 | - |
| | | | 4 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 0 | 7 | F | 0 | - |
| | | | 4-7 | repeat pattern 1...4, use BG[1:0]² = 1, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | | 8-11 | repeat pattern 1...4, use BG[1:0]² = 0, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | | 12-15 | repeat pattern 1...4, use BG[1:0]² = 1, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | | 16-19 | repeat pattern 1...4, use BG[1:0]² = 0, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | | 20-23 | repeat pattern 1...4, use BG[1:0]² = 1, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | | 24-27 | repeat pattern 1...4, use BG[1:0]² = 0, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | | 28-31 | repeat pattern 1...4, use BG[1:0]² = 1, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | | 32-35 | repeat pattern 1...4, use BG[1:0]² = 2, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | | 36-39 | repeat pattern 1...4, use BG[1:0]² = 3, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | | 40-43 | repeat pattern 1...4, use BG[1:0]² = 2, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | | 44-47 | repeat pattern 1...4, use BG[1:0]² = 3, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | | 48-51 | repeat pattern 1...4, use BG[1:0]² = 2, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | |
| | | | 52-55 | repeat pattern 1...4, use BG[1:0]² = 3, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | |
| | | | 56-59 | repeat pattern 1...4, use BG[1:0]² = 2, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | |
| | | | 60-63 | repeat pattern 1...4, use BG[1:0]² = 3, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | |
| | | | 2 | 64 ... nRFC - 1 | repeat Sub-Loop 1, Truncate, if necessary | | | | | | | | | | | | | | | | | |

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

Table 11 - IDD7 Measurement-Loop Pattern¹

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n/A16 | CAS_n/A15 | WE_n/A14 | ODT | C[2:0] ³ | BG[1:0] ² | BA[1:0] | A12/BC_n | A[17,13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data ⁴ | | |
|------------|-------------|-----------------|--|---|--|-------|-----------|-----------|----------|-----|---------------------|----------------------|----------------|----------|-------------|----------|--------|--------|--------|-------------------|--|--|
| toggling | Static High | 0 | 0 | ACT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | |
| | | 1 | 1 | RDA | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF | |
| | | | 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | | 3 | D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3 ² | 3 | 0 | 0 | 0 | 0 | 7 | F | 0 | - |
| | | | ... | repeat pattern 2...3 until nRRD - 1, if nRRD > 4. Truncate if necessary | | | | | | | | | | | | | | | | | | |
| | | | 1 | nRRD | ACT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | nRRD + 1 | RDA | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 |
| | | | ... | repeat pattern 2 ... 3 until 2*nRRD - 1, if nRRD > 4. Truncate if necessary | | | | | | | | | | | | | | | | | | |
| | | | 2 | 2*nRRD | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | |
| | | | 3 | 3*nRRD | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | |
| | | | 4 | 4*nRRD | repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRRD. Truncate if necessary | | | | | | | | | | | | | | | | | |
| | | | 5 | nFAW | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | |
| | | | 6 | nFAW + nRRD | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | |
| | | | 7 | nFAW + 2*nRRD | repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | |
| | | | 8 | nFAW + 3*nRRD | repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | |
| | | | 9 | nFAW + 4*nRRD | repeat Sub-Loop 4 | | | | | | | | | | | | | | | | | |
| | | | 10 | 2*nFAW | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | |
| | | | 11 | 2*nFAW + nRRD | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | |
| | | | 12 | 2*nFAW + 2*nRRD | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | |
| | | | 13 | 2*nFAW + 3*nRRD | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | |
| | 14 | 2*nFAW + 4*nRRD | repeat Sub-Loop 4 | | | | | | | | | | | | | | | | | | | |
| | 15 | 3*nFAW | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead | | | | | | | | | | | | | | | | | | | |
| | 16 | 3*nFAW + nRRD | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 2 instead | | | | | | | | | | | | | | | | | | | |
| | 17 | 3*nFAW + 2*nRRD | repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead | | | | | | | | | | | | | | | | | | | |
| | 18 | 3*nFAW + 3*nRRD | repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 0 instead | | | | | | | | | | | | | | | | | | | |
| | 19 | 3*nFAW + 4*nRRD | repeat Sub-Loop 4 | | | | | | | | | | | | | | | | | | | |
| | 20 | 4*nFAW | repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary | | | | | | | | | | | | | | | | | | | |

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ

IDD Specifications

16GB, 2Gx64 U-DIMM: HMAA2GU6AJR8N

| IDD | | | | | unit | note | IPP | | | | | unit | note |
|--------|------|------|------|------|------|------|--------|------|------|------|------|------|------|
| Symbol | 2400 | 2666 | 2933 | 3200 | | | Symbol | 2400 | 2666 | 2933 | 3200 | | |
| IDD0 | 345 | 359 | 367 | 377 | mA | | IPP0 | 17 | 17 | 17 | 17 | mA | |
| IDD0A | 345 | 359 | 368 | 377 | mA | | IPP1 | 17 | 17 | 17 | 17 | mA | |
| IDD1 | 402 | 418 | 427 | 438 | mA | | IPP2N | 11 | 11 | 11 | 11 | mA | |
| IDD1A | 422 | 442 | 454 | 466 | mA | | IPP2P | 11 | 11 | 11 | 11 | mA | |
| IDD2N | 276 | 287 | 296 | 305 | mA | | IPP3N | 16 | 16 | 16 | 16 | mA | |
| IDD2NA | 276 | 288 | 296 | 306 | mA | | IPP3P | 16 | 16 | 16 | 16 | mA | |
| IDD2NT | 311 | 326 | 338 | 366 | mA | | IPP4R | 16 | 16 | 16 | 16 | mA | |
| IDD2NL | 188 | 197 | 204 | 211 | mA | | IPP4W | 16 | 16 | 16 | 16 | mA | |
| IDD2NG | 272 | 283 | 291 | 300 | mA | | IPP5B | 526 | 526 | 524 | 523 | mA | |
| IDD2ND | 263 | 276 | 284 | 292 | mA | | IPP5F2 | 345 | 346 | 348 | 349 | mA | |
| IDD2NP | 283 | 296 | 305 | 315 | mA | | IPP5F4 | 290 | 283 | 287 | 290 | mA | |
| IDD2P | 183 | 190 | 197 | 203 | mA | | IPP6N | 34 | 34 | 34 | 34 | mA | |
| IDD2Q | 255 | 264 | 270 | 276 | mA | | IPP6E | 58 | 58 | 58 | 58 | mA | |
| IDD3N | 425 | 435 | 443 | 453 | mA | | IPP6R | 18 | 18 | 18 | 18 | mA | |
| IDD3NA | 425 | 435 | 443 | 453 | mA | | IPP6A | 51 | 51 | 51 | 51 | mA | |
| IDD3P | 342 | 345 | 355 | 360 | mA | | IPP7 | 67 | 67 | 67 | 67 | mA | |
| IDD4R | 982 | 1054 | 1137 | 1208 | mA | | IPP8 | 11 | 11 | 11 | 11 | mA | |
| IDD4RA | 999 | 1073 | 1143 | 1216 | mA | | | | | | | | |
| IDD4RB | 995 | 1066 | 1147 | 1220 | mA | | | | | | | | |
| IDD4W | 854 | 907 | 964 | 1019 | mA | | | | | | | | |
| IDD4WA | 878 | 942 | 1003 | 1064 | mA | | | | | | | | |
| IDD4WB | 804 | 859 | 910 | 964 | mA | | | | | | | | |
| IDD4WC | 844 | 903 | 957 | 1018 | mA | | | | | | | | |
| IDD4WP | 1041 | 1112 | 1188 | 1307 | mA | | | | | | | | |
| IDD5B | 3144 | 3145 | 3150 | 3152 | mA | | | | | | | | |
| IDD5F2 | 2169 | 2195 | 2214 | 2235 | mA | | | | | | | | |
| IDD5F4 | 1878 | 1811 | 1856 | 1901 | mA | | | | | | | | |
| IDD6N | 263 | 263 | 263 | 263 | mA | | | | | | | | |
| IDD6E | 395 | 396 | 396 | 396 | mA | | | | | | | | |
| IDD6R | 149 | 149 | 149 | 149 | mA | | | | | | | | |
| IDD6A | 396 | 396 | 396 | 396 | mA | | | | | | | | |
| IDD7 | 1080 | 1123 | 1132 | 1161 | mA | | | | | | | | |
| IDD8 | 112 | 112 | 112 | 112 | mA | | | | | | | | |

32GB, 4Gx64 U-DIMM: HMAA4GU6AJR8N

| IDD | | | | | unit | note | IPP | | | | | unit | note |
|--------|------|------|------|------|------|------|--------|------|------|------|------|------|------|
| Symbol | 2400 | 2666 | 2933 | 3200 | | | Symbol | 2400 | 2666 | 2933 | 3200 | | |
| IDD0 | 617 | 642 | 659 | 678 | mA | | IPP0 | 28 | 28 | 28 | 28 | mA | |
| IDD0A | 617 | 643 | 660 | 679 | mA | | IPP1 | 28 | 28 | 28 | 28 | mA | |
| IDD1 | 674 | 702 | 718 | 739 | mA | | IPP2N | 22 | 22 | 22 | 22 | mA | |
| IDD1A | 694 | 726 | 746 | 767 | mA | | IPP2P | 22 | 22 | 22 | 22 | mA | |
| IDD2N | 548 | 571 | 588 | 607 | mA | | IPP3N | 31 | 31 | 31 | 31 | mA | |
| IDD2NA | 549 | 572 | 589 | 608 | mA | | IPP3P | 31 | 31 | 31 | 31 | mA | |
| IDD2NT | 619 | 648 | 673 | 727 | mA | | IPP4R | 26 | 26 | 26 | 26 | mA | |
| IDD2NL | 373 | 390 | 404 | 418 | mA | | IPP4W | 26 | 26 | 26 | 26 | mA | |
| IDD2NG | 541 | 563 | 579 | 597 | mA | | IPP5B | 536 | 536 | 534 | 533 | mA | |
| IDD2ND | 522 | 548 | 564 | 580 | mA | | IPP5F2 | 355 | 357 | 358 | 360 | mA | |
| IDD2NP | 563 | 588 | 606 | 626 | mA | | IPP5F4 | 301 | 293 | 298 | 301 | mA | |
| IDD2P | 363 | 377 | 390 | 404 | mA | | IPP6N | 68 | 68 | 68 | 68 | mA | |
| IDD2Q | 506 | 525 | 536 | 549 | mA | | IPP6E | 115 | 115 | 115 | 115 | mA | |
| IDD3N | 842 | 862 | 878 | 898 | mA | | IPP6R | 35 | 35 | 35 | 35 | mA | |
| IDD3NA | 841 | 862 | 878 | 898 | mA | | IPP6A | 102 | 102 | 102 | 101 | mA | |
| IDD3P | 677 | 683 | 702 | 713 | mA | | IPP7 | 78 | 78 | 78 | 78 | mA | |
| IDD4R | 1252 | 1336 | 1426 | 1507 | mA | | IPP8 | 22 | 22 | 22 | 22 | mA | |
| IDD4RA | 1270 | 1355 | 1433 | 1515 | mA | | | | | | | | |
| IDD4RB | 1265 | 1347 | 1436 | 1519 | mA | | | | | | | | |
| IDD4W | 1124 | 1189 | 1254 | 1319 | mA | | | | | | | | |
| IDD4WA | 1149 | 1225 | 1294 | 1364 | mA | | | | | | | | |
| IDD4WB | 1074 | 1141 | 1201 | 1263 | mA | | | | | | | | |
| IDD4WC | 1114 | 1185 | 1247 | 1318 | mA | | | | | | | | |
| IDD4WP | 1313 | 1395 | 1479 | 1608 | mA | | | | | | | | |
| IDD5B | 3413 | 3425 | 3438 | 3450 | mA | | | | | | | | |
| IDD5F2 | 2439 | 2476 | 2504 | 2535 | mA | | | | | | | | |
| IDD5F4 | 2148 | 2093 | 2147 | 2201 | mA | | | | | | | | |
| IDD6N | 523 | 523 | 523 | 523 | mA | | | | | | | | |
| IDD6E | 787 | 788 | 789 | 788 | mA | | | | | | | | |
| IDD6R | 296 | 296 | 296 | 294 | mA | | | | | | | | |
| IDD6A | 788 | 788 | 789 | 788 | mA | | | | | | | | |
| IDD7 | 1351 | 1406 | 1423 | 1462 | mA | | | | | | | | |
| IDD8 | 222 | 222 | 222 | 222 | mA | | | | | | | | |

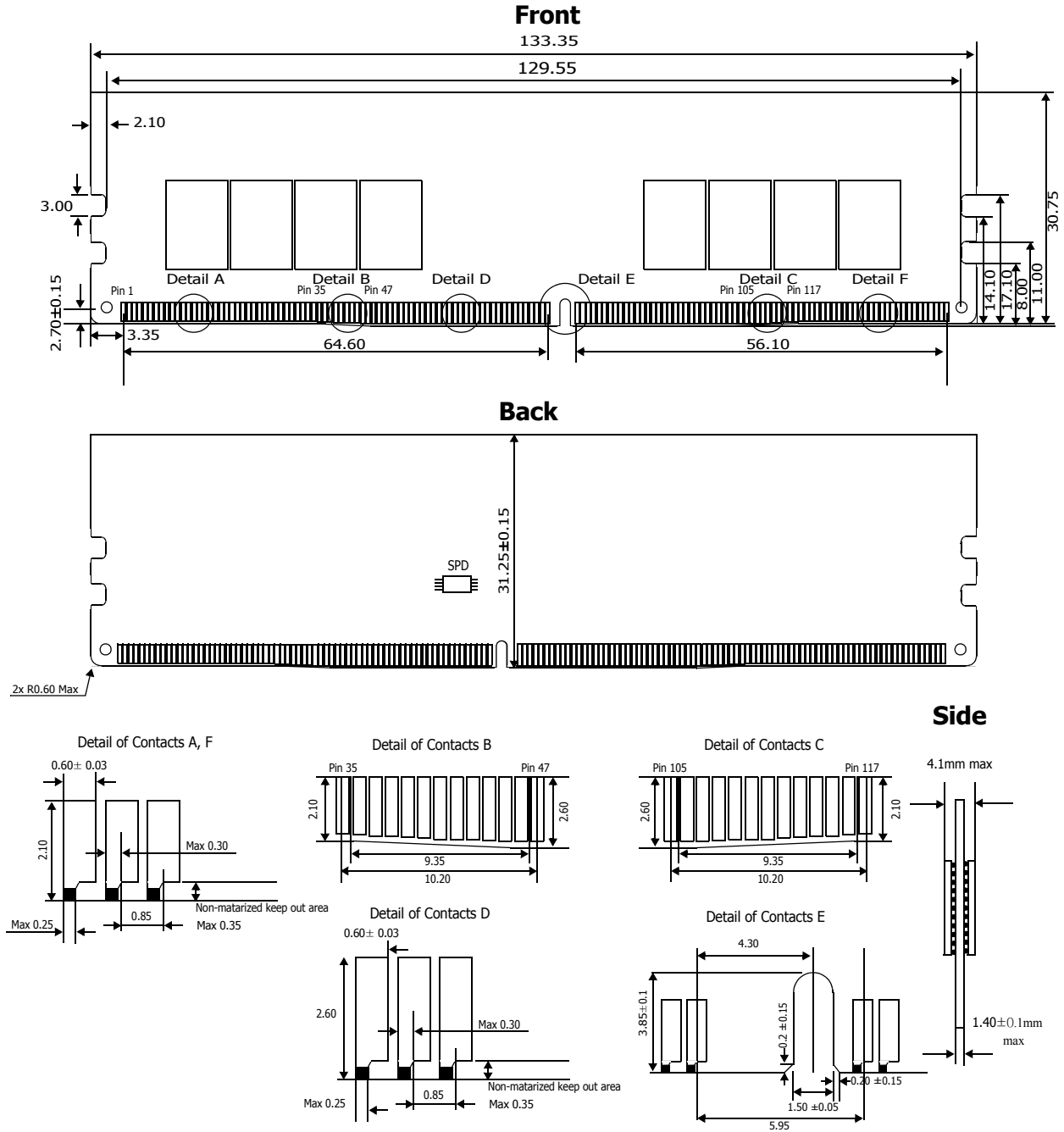
32GB, 4Gx72 U-DIMM: HMAA4GU7AJR8N

| IDD | | | | | unit | note |
|--------|------|------|------|------|------|------|
| Symbol | 2400 | 2666 | 2933 | 3200 | | |
| IDD0 | 694 | 722 | 740 | 762 | mA | |
| IDD0A | 694 | 723 | 742 | 764 | mA | |
| IDD1 | 758 | 789 | 808 | 830 | mA | |
| IDD1A | 781 | 816 | 839 | 863 | mA | |
| IDD2N | 617 | 642 | 661 | 682 | mA | |
| IDD2NA | 617 | 644 | 662 | 684 | mA | |
| IDD2NT | 696 | 729 | 757 | 817 | mA | |
| IDD2NL | 419 | 439 | 455 | 470 | mA | |
| IDD2NG | 608 | 633 | 651 | 671 | mA | |
| IDD2ND | 587 | 616 | 634 | 652 | mA | |
| IDD2NP | 633 | 661 | 682 | 704 | mA | |
| IDD2P | 408 | 424 | 439 | 454 | mA | |
| IDD2Q | 569 | 590 | 603 | 618 | mA | |
| IDD3N | 946 | 969 | 987 | 1009 | mA | |
| IDD3NA | 946 | 969 | 987 | 1009 | mA | |
| IDD3P | 760 | 767 | 789 | 802 | mA | |
| IDD4R | 1408 | 1502 | 1604 | 1695 | mA | |
| IDD4RA | 1428 | 1523 | 1611 | 1704 | mA | |
| IDD4RB | 1423 | 1515 | 1615 | 1708 | mA | |
| IDD4W | 1264 | 1337 | 1410 | 1483 | mA | |
| IDD4WA | 1291 | 1377 | 1455 | 1533 | mA | |
| IDD4WB | 1208 | 1283 | 1350 | 1420 | mA | |
| IDD4WC | 1253 | 1333 | 1403 | 1482 | mA | |
| IDD4WP | 1477 | 1569 | 1664 | 1808 | mA | |
| IDD5B | 3839 | 3852 | 3867 | 3880 | mA | |
| IDD5F2 | 2743 | 2785 | 2817 | 2851 | mA | |
| IDD5F4 | 2416 | 2354 | 2414 | 2475 | mA | |
| IDD6N | 588 | 588 | 588 | 588 | mA | |
| IDD6E | 885 | 887 | 887 | 887 | mA | |
| IDD6R | 332 | 332 | 332 | 331 | mA | |
| IDD6A | 886 | 886 | 887 | 886 | mA | |
| IDD7 | 1520 | 1581 | 1600 | 1644 | mA | |
| IDD8 | 249 | 249 | 249 | 249 | mA | |

| IPP | | | | | unit | note |
|--------|------|------|------|------|------|------|
| Symbol | 2400 | 2666 | 2933 | 3200 | | |
| IPP0 | 31 | 31 | 31 | 31 | mA | |
| IPP1 | 31 | 31 | 31 | 31 | mA | |
| IPP2N | 25 | 25 | 25 | 25 | mA | |
| IPP2P | 25 | 25 | 25 | 25 | mA | |
| IPP3N | 35 | 35 | 35 | 35 | mA | |
| IPP3P | 35 | 35 | 35 | 35 | mA | |
| IPP4R | 30 | 30 | 30 | 30 | mA | |
| IPP4W | 30 | 30 | 30 | 30 | mA | |
| IPP5B | 603 | 603 | 601 | 599 | mA | |
| IPP5F2 | 399 | 401 | 403 | 405 | mA | |
| IPP5F4 | 339 | 330 | 335 | 338 | mA | |
| IPP6N | 76 | 76 | 76 | 76 | mA | |
| IPP6E | 129 | 129 | 129 | 129 | mA | |
| IPP6R | 39 | 39 | 39 | 39 | mA | |
| IPP6A | 114 | 114 | 114 | 114 | mA | |
| IPP7 | 87 | 87 | 87 | 87 | mA | |
| IPP8 | 25 | 25 | 25 | 25 | mA | |

Module Dimensions

2Gx64 - HMAA2GU6AJR8N

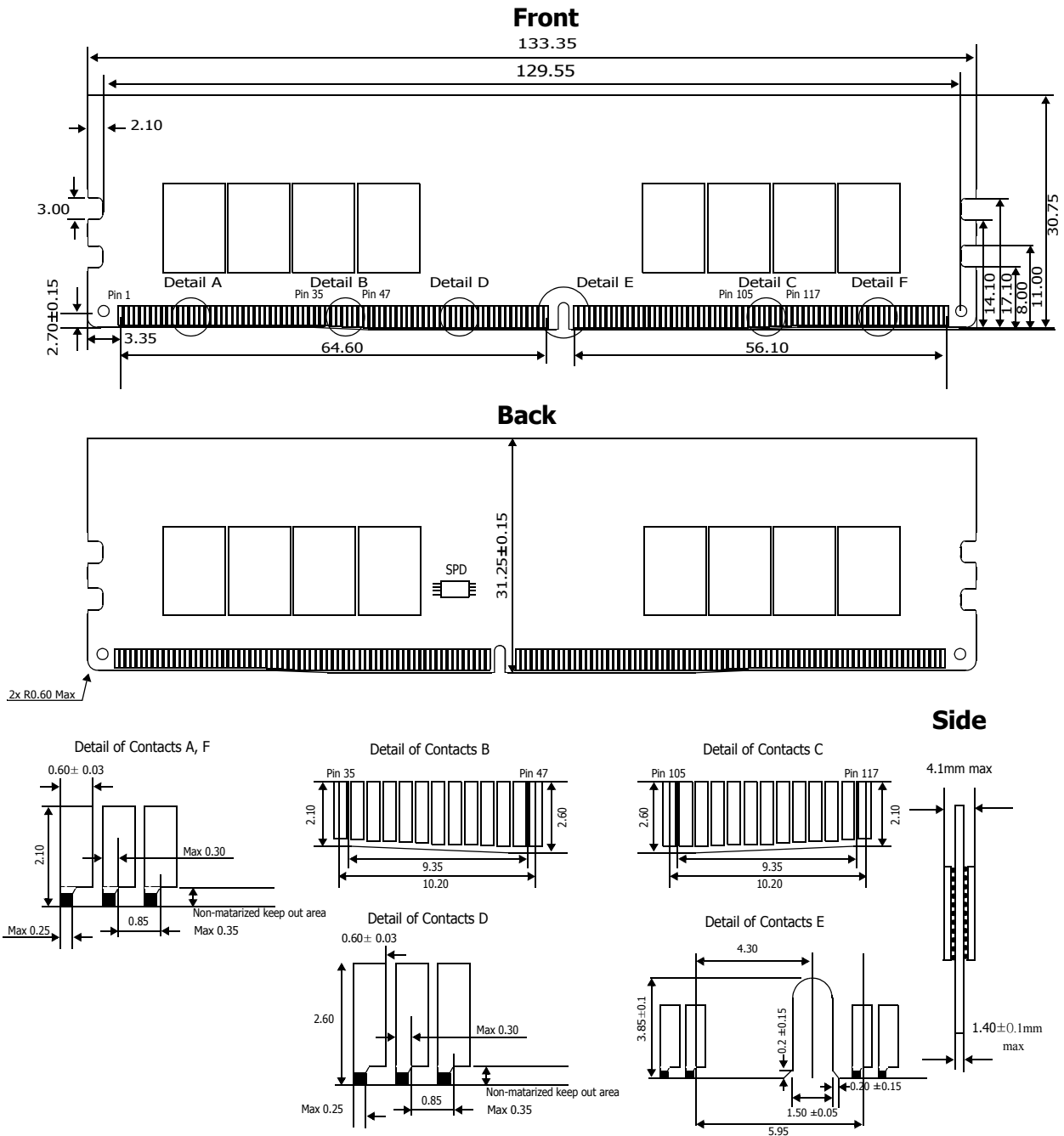


Note:

1. ±0.13 tolerance on all dimensions unless otherwise stated.

Units: millimeters

4Gx64 - HMAA4GU6AJR8N

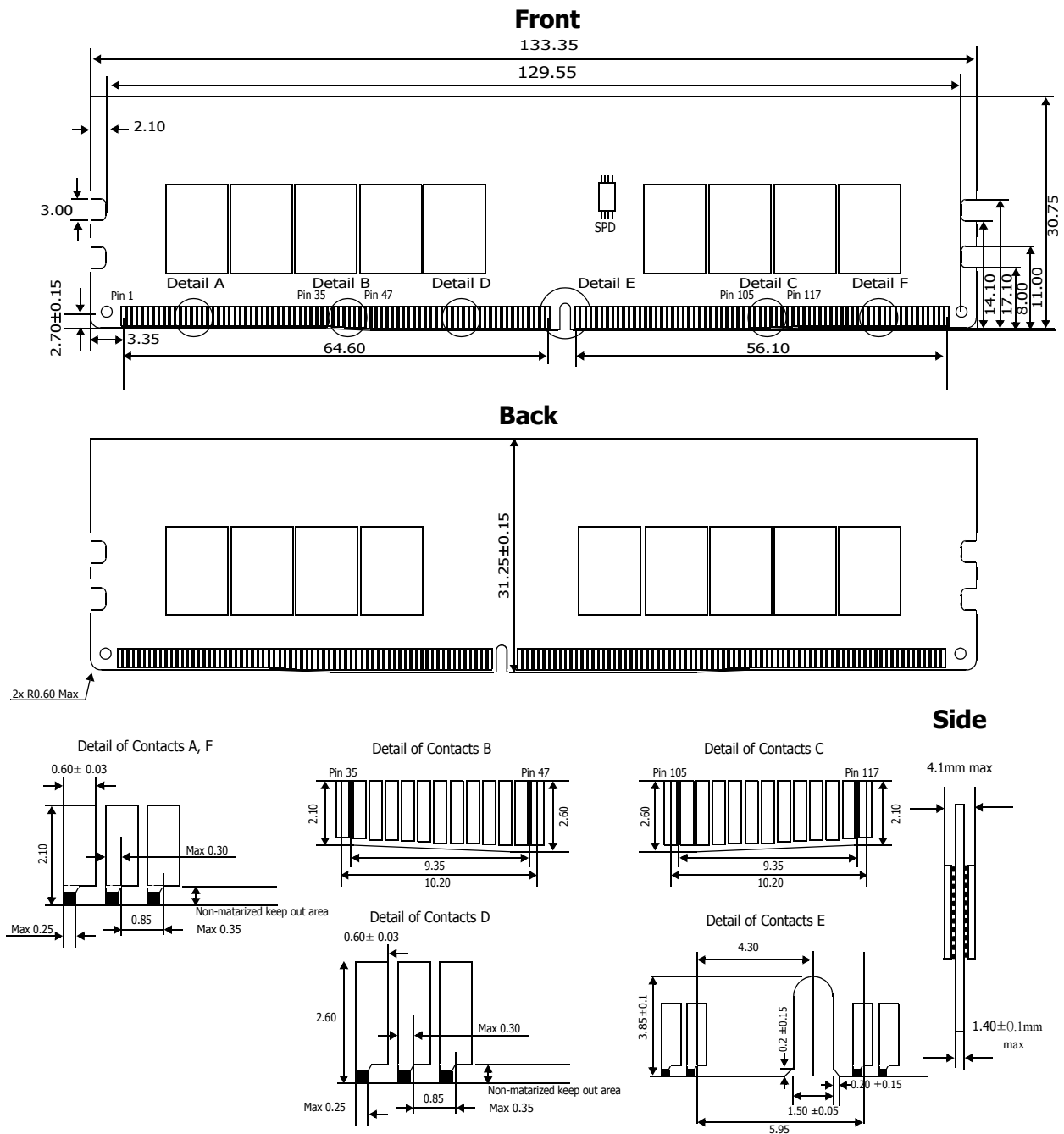


Note:

1. ±0.13 tolerance on all dimensions unless otherwise stated.

Units: millimeters

4Gx72 - HMAA4GU7AJR8N



Note:

1. ±0.13 tolerance on all dimensions unless otherwise stated.

Units: millimeters