

DDR4 SDRAM Registered DIMM Based on 16Gb J-die

**HMAT14JWRRB120N
HMAT14JWRRB122N
HMAT14JXSRB120N
HMAT14JXSRB122N**

***SK hynix reserves the right to change products or specifications without notice.**

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Release	Jul.2020	
0.2	Change 3DS Refresh Specification Correct Ordering Information (Component Part Number)	Oct.2020	
1.0	Define IDD/IPP Specification	Nov.2020	

Description

SK hynix Registered DDR4 SDRAM DIMMs (Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Registered SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

Features

- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP - 2.5V (2.375V to 2.75V)
- VDDSPD=2.25V to 2.75V
- Functionality and operations comply with the DDR4 3DS SDRAM datasheet
- 16 internal banks
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- Data transfer rates: PC4-3200, PC4-2933
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- Supports ECC error correction and detection
- On-Die Termination (ODT)
- Temperature sensor with integrated SPD
- This product is in compliance with the RoHS directive.
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available
- Write CRC is supported at all speed grades
- CA parity (Command/Address Parity) mode is supported

Ordering Information

Part Number	Density	Organization	Component Composition	# of ranks
HMAT14JWRRB120N	256GB	32Gx72	TSV 4Hi 16Gx4(H5AG64JWRDX042N)*36	8
HMAT14JWRRB122N	256GB	32Gx72	TSV 4Hi 16Gx4(H5AG64JWRDX042N)*36	8
HMAT14JXSRB120N	256GB	32Gx72	TSV 4Hi 16Gx4(H5AG64JXSDX042N)*36	8
HMAT14JXSRB122N	256GB	32Gx72	TSV 4Hi 16Gx4(H5AG64JXSDX042N)*36	8

Key Parameters

MT/s	Grade	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR4-2933	-WR	0.682	24	14.32	14.32	32	46.32	24-21-21
DDR4-3200	-XS	0.625	26	13.75	13.75	32	47.00	26-22-22

*SK hynix DRAM devices support optional downbinning to CL20, CL22, CL24 and CL26. SPD setting is programm

Address Table

		256GB(8Rx4)
Rank Address		CS0, CS1
Chip ID		C0, C1
Bank Address	# of Bank Groups	4
	BG Address	BG0~BG1
	Bank Address in a BG	BA0~BA1
Row Address		A0~A17
Column Address		A0~ A9
Page size		512B

Pin Descriptions

Pin Name	Description	Pin Name	Description
A0-A17 ¹	Register address input	SCL	I ² C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I ² C serial data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0-SA2	I ² C slave address select for SPD-TSE and register
RAS _n ²	Register row address strobe input	PAR	Register parity input
CAS _n ³	Register column address strobe input	VDD	SDRAM core power supply
WE _n ⁴	Register write enable input	C0, C1, C2	Chip ID lines for SDRAMx
CS0 _n , CS1 _n , CS2 _n , CS3 _n	DIMM Rank Select Lines input	12V	Optional Power Supply on socket but not used on RDIMM
CKE0, CEK1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT _n	Register input for activate input	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT _n	Register ALERT _n output
CB0-CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9 _t -TDQS17 _t TDQS9 _c -TDQS17 _c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0 _t -DQS17 _t	Data Buffer data strobes (positive line of differential pair)	DM0 _n -DM8 _n	Data Mask
DQS0 _c -DQS17 _c	Data Buffer data strobes (negative line of differential pair)	RESET _n	Set Register and SDRAMs to a Known State
DBI0 _n -DBI8 _n	Data Bus Inversion	EVENT _n	SPD signals a thermal event has occurred
CK0 _t , CK1 _t	Register clock input (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0 _c , CK1 _c	Register clocks input (negative line of differential pair)	RFU	Reserved for future use

1. Address A17 is only valid for 16Gbx4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Input/Output Functional Descriptions

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, TDQS_t, and TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15, and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command being entered. Those pins are multi-function. For example, for activation with ACT_n Low, these are Addresses like A16, A15, and A14, but for non-activation command with ACT_n High, these are Command pins for Read, Write, and other commands defined in command truth table.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16Gb x4 SDRAM configurations.

Symbol	Type	Function
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS9_t-TDQS17_t, TDQS9_c-TDQS17_c	Input	Provides a dummy load for x8 based RDIMMs where mixed populations of x4 and x8 based RDIMMs are present.
DBI0_n-DBI8_n	Input/ Output	Provides for data bus inversion. Only possible for x8 based RDIMMs and where only x8 based RDIMMs are on a channel.
DM0_n-DM8_n	Input	Provides for masking of a byte on WRITE commands to the SDRAMs. Only Possible x8 based RDIMMs and where only x8 based RDIMMs are on a channel.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time as command & address, with CS_n LOW.
ALERT_n	Output (Input)	Alert: Is multi functions, such as CRC error flag or Command and Address Parity error flag, as on Output signal. If there is an error in the CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is an error in the Command Address Parity Check, then ALERT_n goes LOW for a relatively long period until on going SDRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input. Using this signal or not is dependent on the system.
RFU		Reserved for Future Use: No on-DIMM electrical connection is present.
NC		No Connect: No on-DIMM electrical connection is present.
VDD ¹	Supply	Power Supply: 1.2 V ± 0.06 V
VSS	Supply	Ground

Symbol	Type	Function
VTT	Supply	Power Supply for termination of Address, Command and Control, VDD/2.
12V	Supply	12V supply not used on RDIMMs.
VPP	Supply	SDRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD-TSE and register.
VREFCA	Supply	Reference voltage for CA

Note: For PC4, VDD is 1.2V. For PC4L, VDD is TBD.

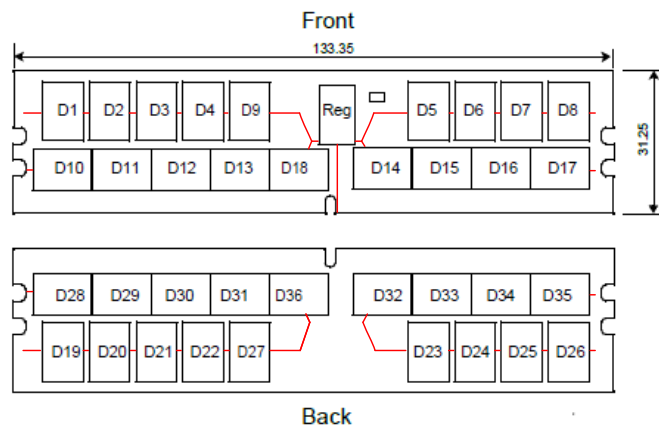
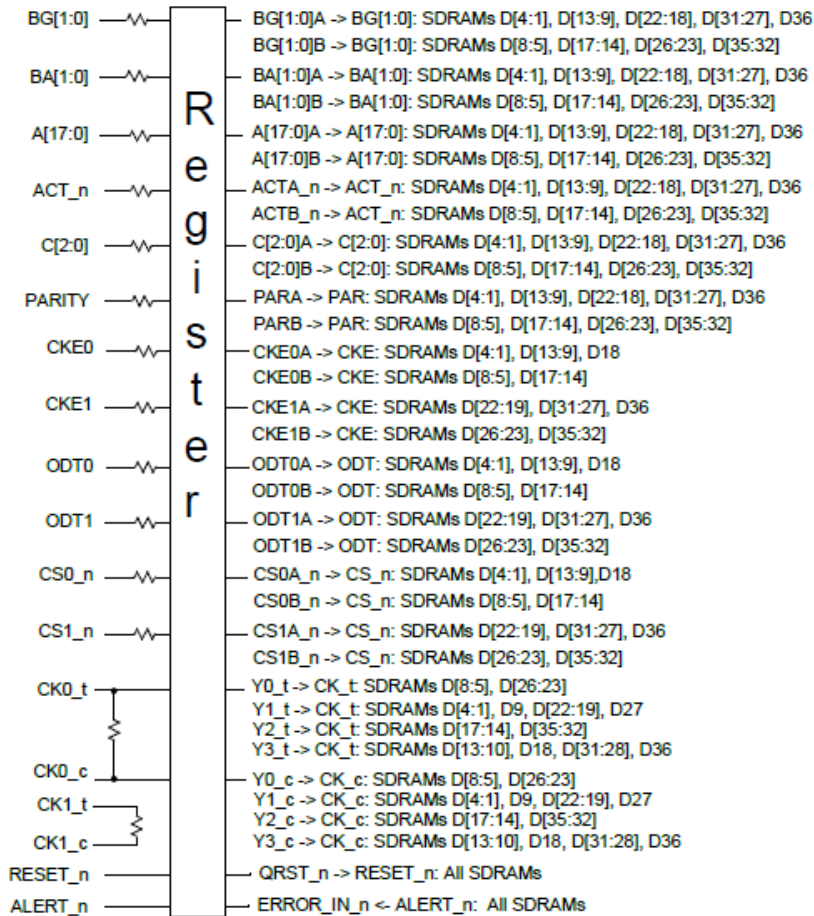
Pin Assignments

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
1	NC	145	NC	74	CK0_t	218	CK1_t
2	VSS	146	VREFCA	75	CK0_c	219	CK1_c
3	DQ4	147	VSS	76	VDD	220	VDD
4	VSS	148	DQ5	77	VTT	221	VTT
5	DQ0	149	VSS	KEY			
6	VSS	150	DQ1				
7	TDQS9_t, DQS9_t, DM0_n, DBI0_n	151	VSS	78	EVENT_n	222	PARITY
8	TDQS9_c, DQS9_c	152	DQS0_c	79	A0	223	VDD
9	VSS	153	DQS0_t	80	VDD	224	BA1
10	DQ6	154	VSS	81	BA0	225	A10/AP
11	VSS	155	DQ7	82	RAS_n/A16	226	VDD
12	DQ2	156	VSS	83	VDD	227	RFU
13	VSS	157	DQ3	84	CS0_n	228	WE_n/A14
14	DQ12	158	VSS	85	VDD	229	VDD
15	VSS	159	DQ13	86	CAS_n/A15	230	NC
16	DQ8	160	VSS	87	ODT0	231	VDD
17	VSS	161	DQ9	88	VDD	232	A13
18	TDQS10_t, DQS10_t, DM1_n, DBI1_n	162	VSS	89	CS1_n, NC	233	VDD
19	TDQS10_c, DQS10_c	163	DQS1_c	90	VDD	234	A17
20	VSS	164	DQS1_t	91	ODT1, NC	235	NC, C2
21	DQ14	165	VSS	92	VDD	236	VDD
22	VSS	166	DQ15	93	C0, CS2_n, NC	237	NC, CS3_n, C1
23	DQ10	167	VSS	94	VSS	238	SA2
24	VSS	168	DQ11	95	DQ36	239	VSS
25	DQ20	169	VSS	96	VSS	240	DQ37
26	VSS	170	DQ21	97	DQ32	241	VSS
27	DQ16	171	VSS	98	VSS	242	DQ33
28	VSS	172	DQ17	99	TDQS13_t, DQS13_t, DM4_n, DBI4_n	243	VSS
29	TDQS11_t, DQS11_t, DM2_n, DBI2_n	173	VSS	100	TDQS13_c, DQS13_c	244	DQS4_c
30	TDQS11_c, DQS11_c	174	DQS2_c	101	VSS	245	DQS4_t
31	VSS	175	DQS2_t	102	DQ38	246	VSS
32	DQ22	176	VSS	103	VSS	247	DQ39
33	VSS	177	DQ23	104	DQ34	248	VSS
34	DQ18	178	VSS	105	VSS	249	DQ35
35	VSS	179	DQ19	106	DQ44	250	VSS
36	DQ28	180	VSS	107	VSS	251	DQ45

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
37	VSS	181	DQ29	108	DQ40	252	VSS
38	DQ24	182	VSS	109	VSS	253	DQ41
39	VSS	183	DQ25	110	TDQS14_t, DQS14_t, DM5_n, DBI5_n	254	VSS
40	TDQS12_t, DQS12_t, DM3_n, DBI3_n	184	VSS	111	TDQS14_c, DQS14_c	255	DQS5_c
41	TDQS12_c, DQS12_c	185	DQS3_c	112	VSS	256	DQS5_t
42	VSS	186	DQS3_t	113	DQ46	257	VSS
43	DQ30	187	VSS	114	VSS	258	DQ47
44	VSS	188	DQ31	115	DQ42	259	VSS
45	DQ26	189	VSS	116	VSS	260	DQ43
46	VSS	190	DQ27	117	DQ52	261	VSS
47	CB4	191	VSS	118	VSS	262	DQ53
48	VSS	192	CB5	119	DQ48	263	VSS
49	CB0	193	VSS	120	VSS	264	DQ49
50	VSS	194	CB1	121	TDQS15_t, DQS15_t, DM6_n, DBI6_n	265	VSS
51	TDQS17_t, DQS17_t, DM8_n, DBI8_n	195	VSS	122	TDQS15_c, DQS15_c	266	DQS6_c
52	TDQS17_c, DQS17_c	196	DQS8_c	123	VSS	267	DQS6_t
53	VSS	197	DQS8_t	124	DQ54	268	VSS
54	CB6	198	VSS	125	VSS	269	DQ55
55	VSS	199	CB7	126	DQ50	270	VSS
56	CB2	200	VSS	127	VSS	271	DQ51
57	VSS	201	CB3	128	DQ60	272	VSS
58	RESET_n	202	VSS	129	VSS	273	DQ61
59	VDD	203	CKE1, NC	130	DQ56	274	VSS
60	CKE0	204	VDD	131	VSS	275	DQ57
61	VDD	205	RFU	132	TDQS16_t, DQS16_t, DM7_n, DBI7_n	276	VSS
62	ACT_n	206	VDD	133	TDQS16_t, DQS16_c	277	DQS7_c
63	BG0	207	BG1	134	VSS	278	DQS7_t
64	VDD	208	ALERT_n	135	DQ62	279	VSS
65	A12/BC_n	209	VDD	136	VSS	280	DQ63
66	A9	210	A11	137	DQ58	281	VSS
67	VDD	211	A7	138	VSS	282	DQ59
68	A8	212	VDD	139	SA0	283	VSS
69	A6	213	A5	140	SA1	284	VDDSPD
70	VDD	214	A4	141	SCL	285	SDA
71	A3	215	VDD	142	VPP	286	VPP
72	A1	216	A2	143	VPP	287	VPP
73	VDD	217	VDD	144	RFU	288	VPP

Functional Block Diagram

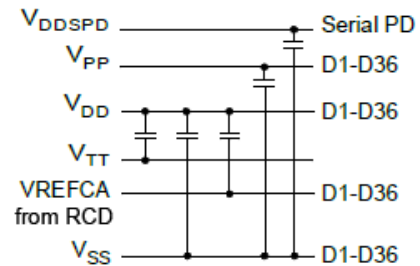
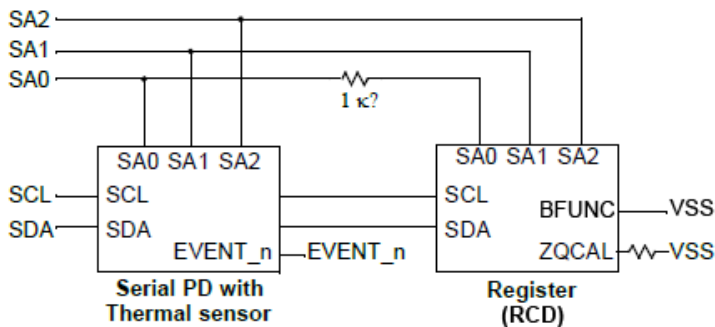
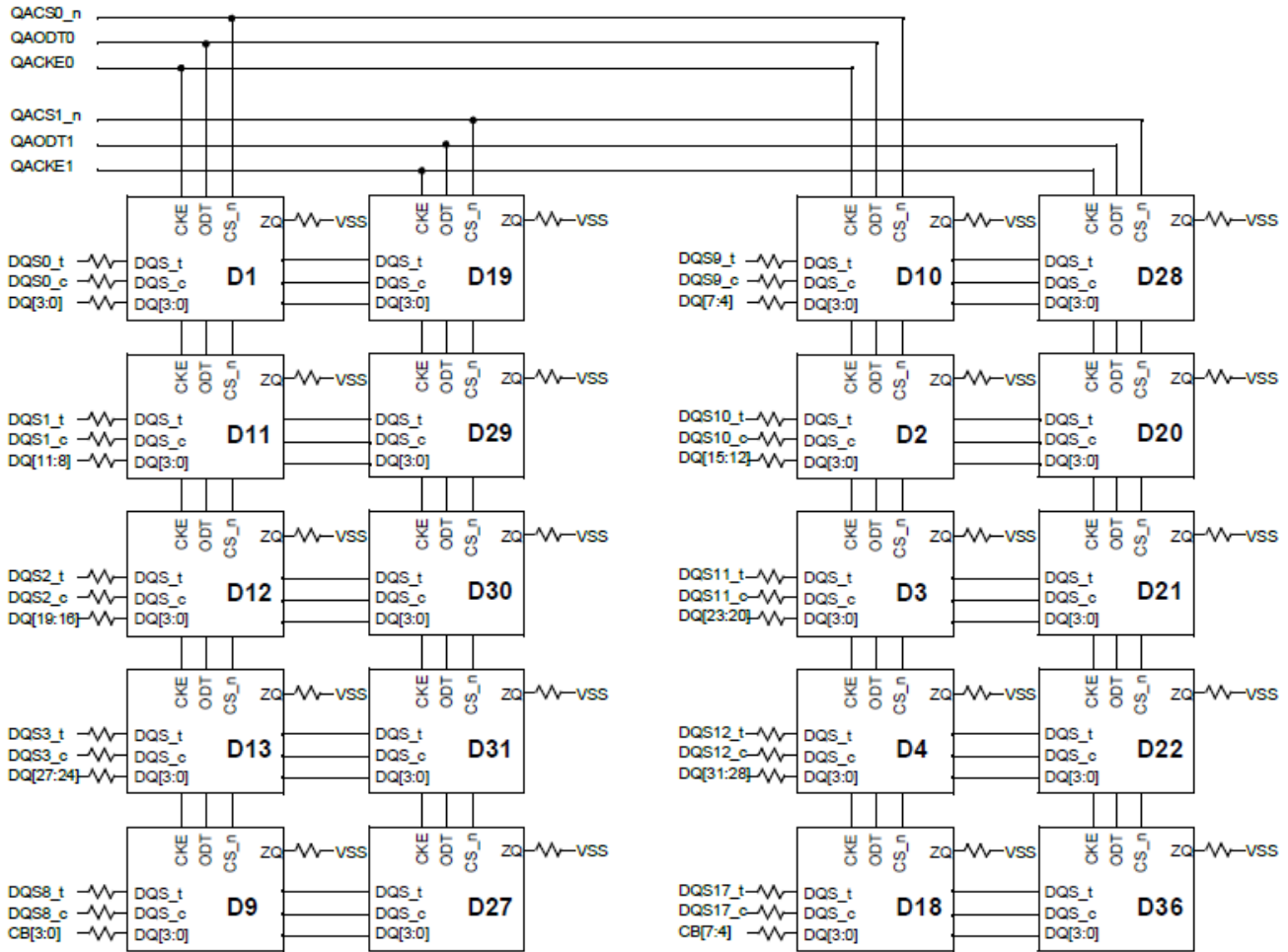
256GB, 32Gx72 Module(2Rank of x4) - Part 1 of 3



Note:

1. CK0_t, CK0_c terminated with 120 Ω±5% resistor.
2. CK1_t, CK1_c terminated with 120 Ω±5% resistor but not used.
3. Unless otherwise noted resistors are 22 Ω±5% . .

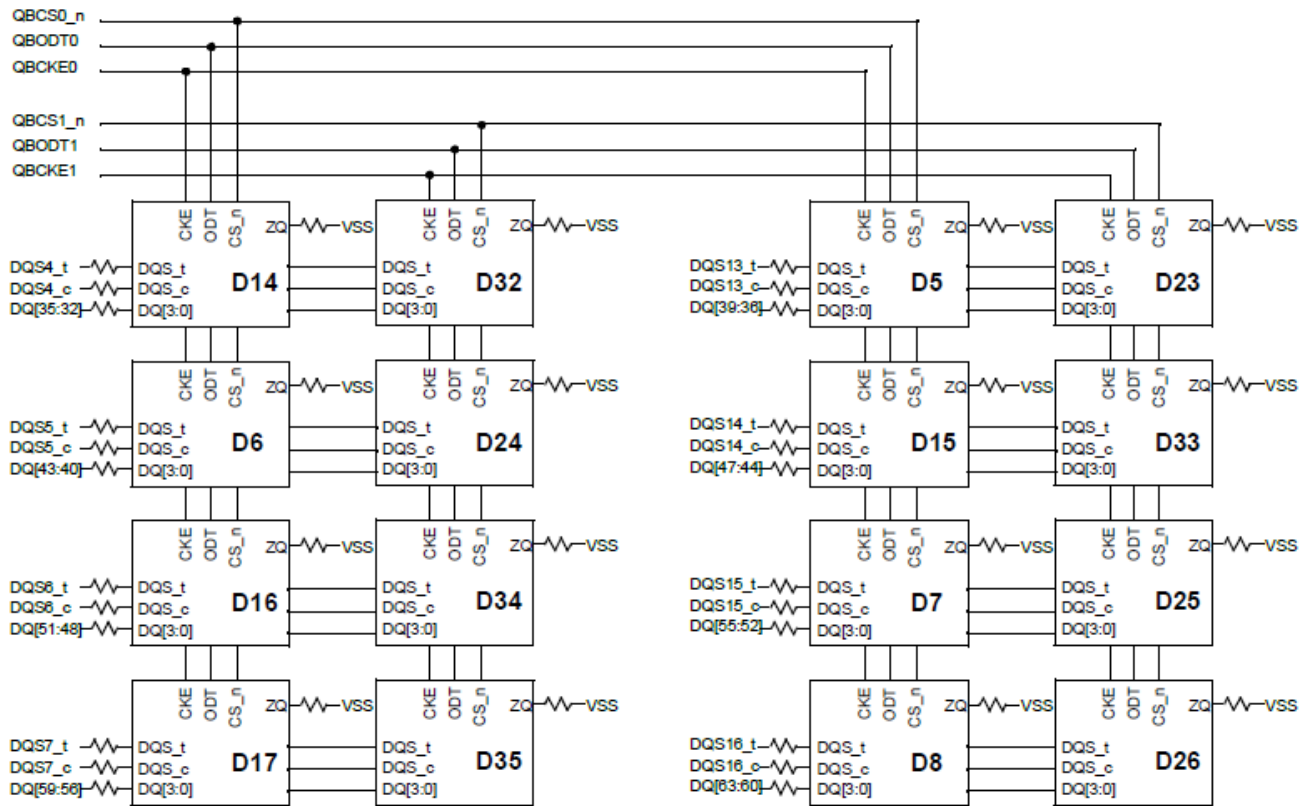
256GB, 32Gx72 Module(2Rank of x4) - Part 2 of 3



Note:

1. Unless otherwise noted, resistor values are $15\ \Omega \pm 5\%$.
2. See the Net Structure diagrams for all resistor associated with the command, address and control bus.
3. ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.
4. DRAM TEN pin need to be tied to VSS.
5. VDDSPD also connects to the register (RCD).
6. VREFCA from the edge connector only connects with the register (RCD). The RCD sources a separate VREFCA to all the SDRAMs.

256GB, 32Gx72 Module(2Rank of x4) - Part 3 of 3



Absolute Maximum Ratings

Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V _{IN} , V _{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3,5
T _{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
- VPP must be equal or greater than VDD/VDDQ at all times
- Overshoot area above 1.5V is specified in DDR4 Device Operation.

DRAM Component Operating Temperature Range

Temperature Range

Symbol	Parameter	Rating	Units	Notes
T _{OPER}	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range	85 to 95	°C	1,3

NOTE:

- Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

AC & DC Operating Conditions

Recommended DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

NOTE:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

AC & DC Input Measurement Levels

AC & DC Logic input levels for single-ended signals

Single-ended AC & DC input levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/ 2400		DDR4-2666/2933/3200		Unit	NOTE
		Min.	Max.	Min.	Max.		
$V_{IH.CA}(DC75)$	DC input logic high	$V_{REFCA} + 0.075$	VDD	-	-	V	
$V_{IL.CA}(DC75)$	DC input logic low	VSS	$V_{REFCA} - 0.075$	-	-	V	
$V_{IH.CA}(DC65)$	DC input logic high	-	-	$V_{REFCA} + 0.065$	VDD	V	
$V_{IL.CA}(DC65)$	DC input logic low	-	-	Note 2	$V_{REF} - 0.09$	V	
$V_{IH.CA}(AC100)$	AC input logic high	$V_{REF} + 0.1$	Note 2	-	-	V	1
$V_{IL.CA}(AC100)$	AC input logic low	Note 2	$V_{REF} - 0.1$	-	-	V	1
$V_{IH.CA}(AC90)$	AC input logic high	-	-	$V_{REF} + 0.09$	Note 2	V	1
$V_{IL.CA}(AC90)$	AC input logic low	-	-	Note 2	$V_{REF} - 0.09$	V	1
$V_{REFCA}(DC)$	Reference Voltage for ADD, CMD inputs	$0.49 * VDD$	$0.51 * VDD$	$0.49 * VDD$	$0.51 * VDD$	V	2,3

NOTE :

1. See "Overshoot and Undershoot Specifications" on section 8.3.
2. The AC peak noise on V_{REFCA} may not allow V_{REFCA} to deviate from $V_{REFCA}(DC)$ by more than $\pm 1\%$ VDD (for reference : approx. $\pm 12mV$)
3. For reference : approx. $VDD/2 \pm 12mV$

AC and DC Input Measurement Levels: V_{REF} Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure below. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA}).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than $\pm 1\% V_{DD}$.

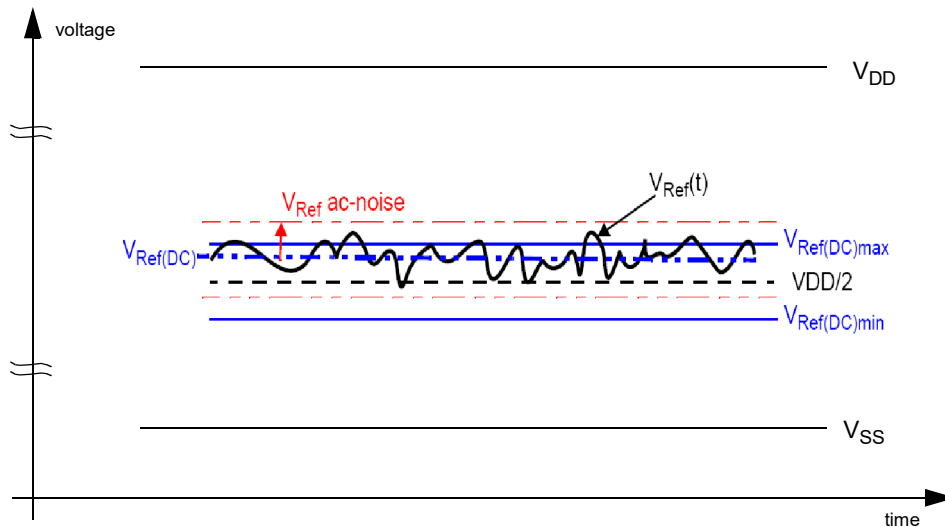


Illustration of $V_{REF}(DC)$ tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF} .

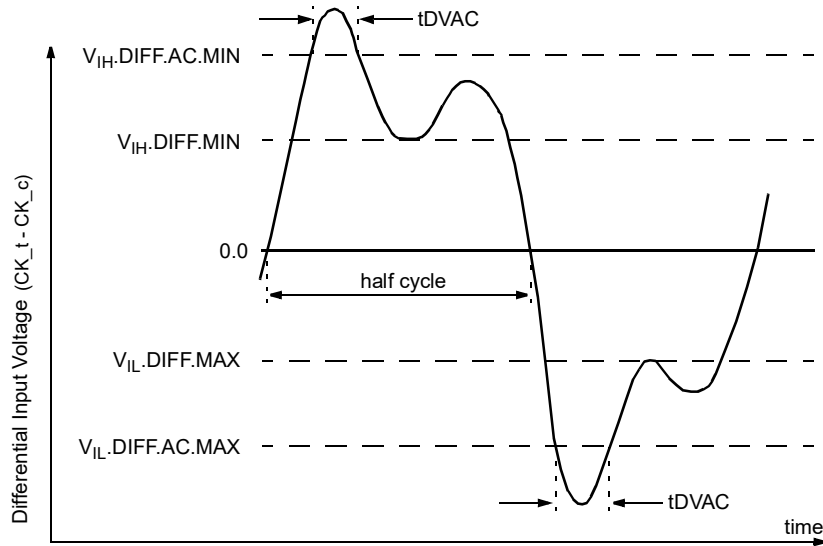
" V_{REF} " shall be understood as $V_{REF}(DC)$, as defined in Figure above.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit ($\pm 1\%$ of V_{DD}) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signal definition



NOTE:

1. Differential signal rising edge from $V_{IL.DIFF.MAX}$ to $V_{IH.DIFF.MIN}$ must be monotonic slope.
2. Differential signal falling edge from $V_{IH.DIFF.MIN}$ to $V_{IL.DIFF.MAX}$ must be monotonic slope.

Definition of differential ac-swing and "time above ac-level" t_{DVAC}

Differential swing requirements for clock (CK_t - CK_c) Differential AC and DC Input Levels

Symbol	Parameter	DDR4 - 1600,1866,2133		DDR4 -2400		DDR4 -2666		DDR4 -2933		DDR4 -3200		unit	NOTE
		min	max	min	max	min	max	min	max	min	max		
V _{IHdiff}	differential input high	+0.150	NOTE 3	+0.135	NOTE 3	+0.135	NOTE 3	+0.125	NOTE 3	+0.110	NOTE 3	V	1
V _{ILdiff}	differential input low	NOTE 3	-0.150	NOTE 3	-0.135	NOTE 3	-0.135	NOTE 3	-0.125	NOTE 3	-0.110	V	1

NOTE :

- Used to define a differential signal slew-rate.
- for CK_t - CK_c use V_{IH.CA}/V_{IL.CA}(AC) of ADD/CMD and V_{REFCA};
- These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits (V_{IH.CA}(DC) max, V_{IL.CA}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Allowed time before ringback (tDVAC) for CK_t - CK_c

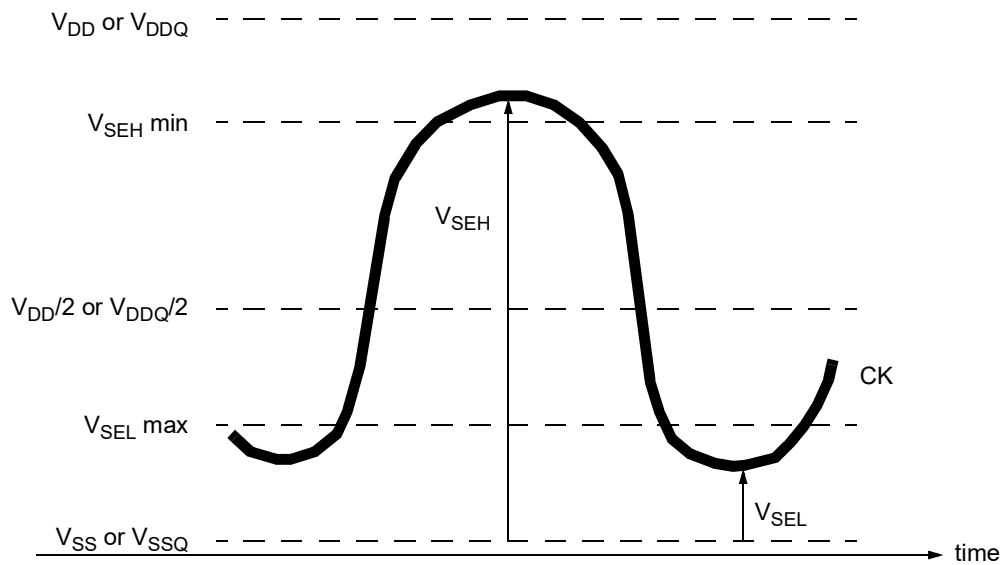
Slew Rate [V/ns]	tDVAC [ps] @ V _{IH/Ldiff} (AC) = 200mV		tDVAC [ps] @ V _{IH/Ldiff} (AC) = TBDmV	
	min	max	min	max
> 4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
< 1.0	80	-	TBD	-

Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach V_{SEH}min / V_{SEL}max (approximately equal to the ac-levels (V_{IH.CA(AC)} / V_{IL.CA(AC)}) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than V_{IH.CA(AC100)}/V_{IL.CA(AC100)} is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c



Single-ended requirement for differential signals

Note that, while ADD/CMD signal requirements are with respect to V_{refCA}, the single-ended components of differential signals have a requirement with respect to V_{DD} / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SEL}max, V_{SEH}min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK_t, CK_c

Symbol	Parameter	DDR4-1600/ 1866/2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
V _{SEH}	Single-ended high-level for CK_t, CK_c	(VDD/2)+0.100	NOTE3	(VDD/2)+0.095	NOTE3	(VDD/2)+0.095	NOTE3	(VDD/2)+0.085	NOTE3	(VDD/2)+0.085	NOTE3	V	1, 2
V _{SEL}	Single-ended low-level for CK_t, CK_c	NOTE3	(VDD/2)-0.100	NOTE3	(VDD/2)-0.095	NOTE3	(VDD/2)-0.095	NOTE3	(VDD/2)-0.085	NOTE3	(VDD/2)-0.085	V	1, 2

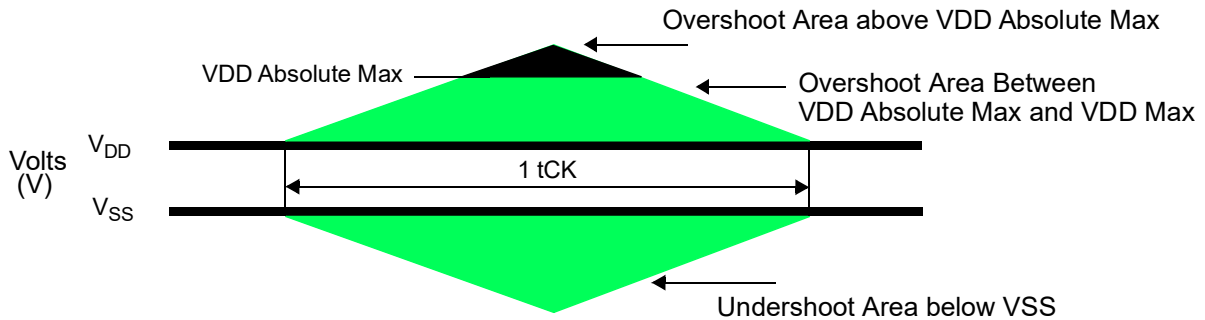
NOTE :

1. For CK_t - CK_c use V_{IH.CA}/V_{IL.CA}(AC) of ADD/CMD;
2. V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};
3. These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits (V_{IH.CA}(DC) max, V_{IL.CA}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Address and Control Overshoot and Undershoot specifications

AC overshoot/undershoot specification for Address, Command and Control pins

Parameter	Specification							Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	
Maximum peak amplitude above VDD Absolute Max allowed for overshoot area	0.06				0.06			V
Delta value between VDD Absolute Max and VDD Max allowed for overshoot area	VDD + 0.24				VDD + 0.24			V
Maximum peak amplitude allowed for undershoot area	0.30				0.30			V-ns
Maximum overshoot area per 1tCK Above Absolute Max	0.0083	0.0071	0.0062	0.0055	0.0055			V-ns
Maximum overshoot area per 1tCK Between Absolute Max	0.2550	0.2185	0.1914	0.1699	0.1699			V-ns
Maximum undershoot area per 1tCK Below VSS	0.2644	0.2265	0.1984	0.1762	0.1762			V-ns
(A0-A13,A17,BG0-BG1,BA0-BA1,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT,C2-C0)								

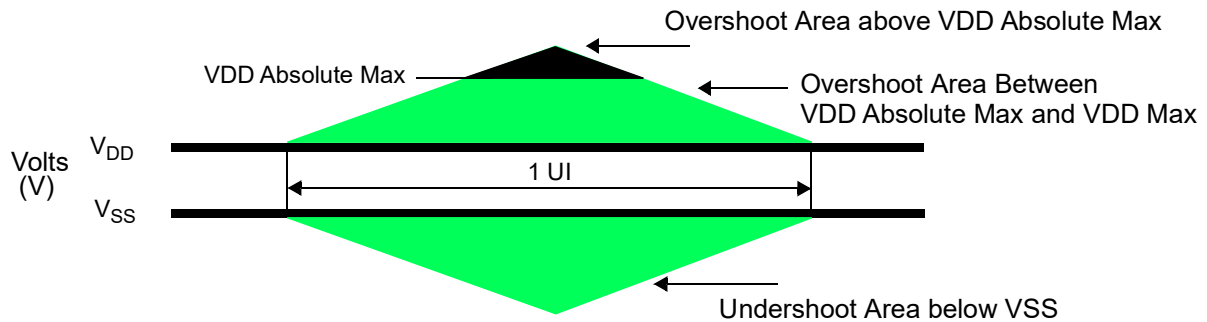


Address,Command and Control Overshoot and Undershoot Definition

Clock Overshoot and Undershoot Specifications

AC overshoot/undershoot specification for Clock

Parameter	Specification							Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	
Maximum peak amplitude above VDD Absolute Max allowed for overshoot area	0.06				0.06			V
Delta value between VDD Absolute Max and VDD Max allowed for overshoot area	VDD + 0.24				VDD + 0.24			V
Maximum peak amplitude allowed for undershoot area	0.30				0.30			V
Maximum overshoot area per 1UI Above Absolute Max	0.0038	0.0032	0.0028	0.0025	0.0025		V-ns	
Maximum overshoot area per 1UI Between Absolute Max	0.1125	0.0964	0.0844	0.0750	0.0750		V-ns	
Maximum undershoot area per 1UI Below VSS	0.1144	0.0980	0.0858	0.0762	0.0762		V-ns	
(CK _t , Ck _c)								



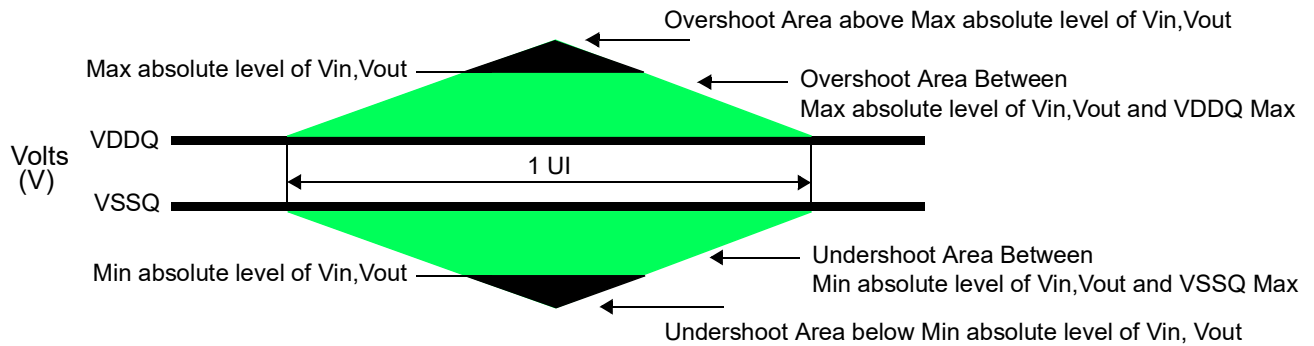
Clock Overshoot and Undershoot Definition

Data, Strobe and Mask Overshoot and Undershoot Specifications

AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	Specification							Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	
Maximum peak amplitude above Max absolute level of Vin,Vout	0.16	0.16	0.16	0.16	0.16			V
Overshoot area Between Max Absolute level of Vin, Vout and VDDQ Max	VDDQ + 0.24				VDDQ+0.24			V
Undershoot area Between Min absolute level of Vin,Vout and VDDQ Max	0.30	0.30	0.30	0.30	0.30			V
Maximum peak amplitude below Min absolute level of Vin,Vout	0.10	0.10	0.10	0.10	0.10			V
Maximum overshoot area per 1UI Above Max absolute level of Vin,Vout	0.0150	0.0129	0.0113	0.0100	0.0100			V-ns
Maximum overshoot area per 1UI Between Max absolute level of Vin,Vout and VDDQ Max	0.1050	0.0900	0.0788	0.0700	0.0700			V-ns
Maximum undershoot area per 1UI Between Min absolute level of Vin,Vout and VSSQ	0.1050	0.0900	0.0788	0.0700	0.0700			V-ns
Maximum undershoot area per 1UI Below Min absolute level of Vin,Vout	0.0150	0.0129	0.0113	0.0100	0.0100			V-ns

(DQ, DQS_t, DQS_c, DM_n, DBI_n, TDQS_t, TDQS_c)



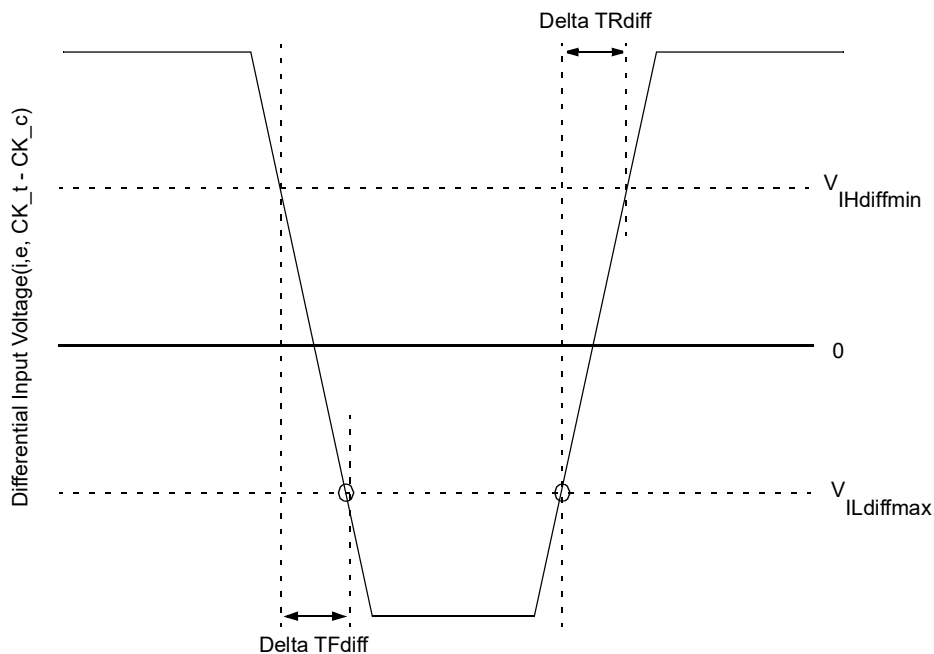
Slew Rate Definitions

Slew Rate Definitions for Differential Input Signals (CK)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Table and Figure below.

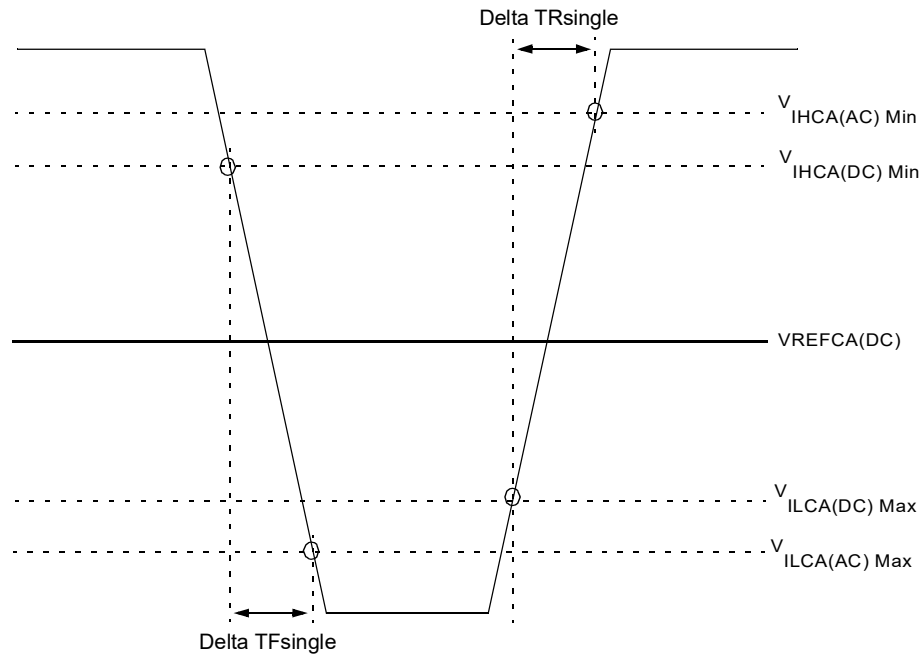
Differential Input Slew Rate Definition

Description			Defined by
	from	to	
Differential input slew rate for rising edge(CK _t - CK _c)	V _{ILdiffmax}	V _{IHdiffmin}	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TR_{diff}$
Differential input slew rate for falling edge(CK _t - CK _c)	V _{IHdiffmin}	V _{ILdiffmax}	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TF_{diff}$
NOTE: The differential signal (i.e.,CK _t - CK _c) must be linear between these thresholds.			



Differential Input Slew Rate Definition for CK_t, CK_c

Slew Rate Definition for Single-ended Input Signals (CMD/ADD)



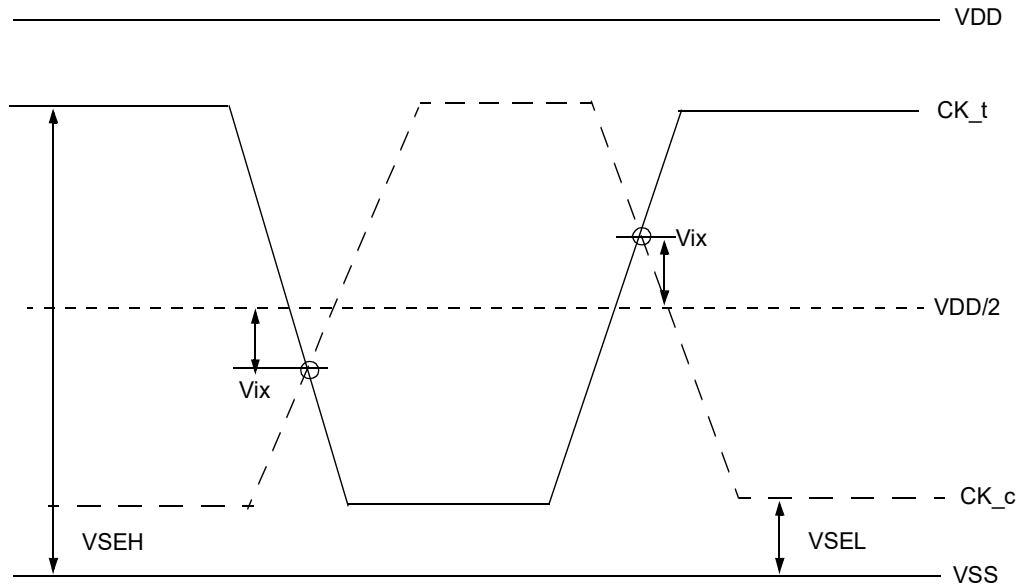
Single-ended Input Slew Rate definition for CMD and ADD

NOTE :

1. Single-ended input slew rate for rising edge = $\{ V_{IHCA(AC)Min} - V_{ILCA(DC)Max} \} / \Delta T_{Rsingle}$
2. Single-ended input slew rate for falling edge = $\{ V_{IHCA(DC)Min} - V_{ILCA(AC)Max} \} / \Delta T_{Fsingle}$
3. Single-ended signal rising edge from $V_{ILCA(DC)Max}$ to $V_{IHCA(DC)Min}$ must be monotonic slope.
4. Single-ended signal falling edge from $V_{IHCA(DC)Min}$ to $V_{ILCA(DC)Max}$ must be monotonic slope

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.



Vix Definition (CK)

Cross point voltage for differential input signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133/2400			
		min		max	
-	Area of VSEH, VSEL	$VSEL \leq VDD/2 - 145mV$	$VDD/2 - 145mV \leq VSEL \leq VDD/2 - 100mV$	$VDD/2 + 100mV \leq VSEL \leq VDD/2 + 145mV$	$VDD/2 + 145mV \leq VSEL$
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-120mV	$-(VDD/2 - VSEL) + 25mV$	$(VSEH - VDD/2) - 25mV$	120mV

Symbol	Parameter	DDR4-2666/2933/3200			
		min		max	
-	Area of VSEH, VSEL	$VSEL \leq VDD/2 - 145mV$	$VDD/2 - 145mV \leq VSEL \leq VDD/2 - 100mV$	$VDD/2 + 100mV \leq VSEH \leq VDD/2 + 145mV$	$VDD/2 + 145mV \leq VSEH$
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-110mV	$-(VDD/2 - VSEL) + 30mV$	$(VSEH - VDD/2) - 30mV$	110mV

CMOS rail to rail Input Levels

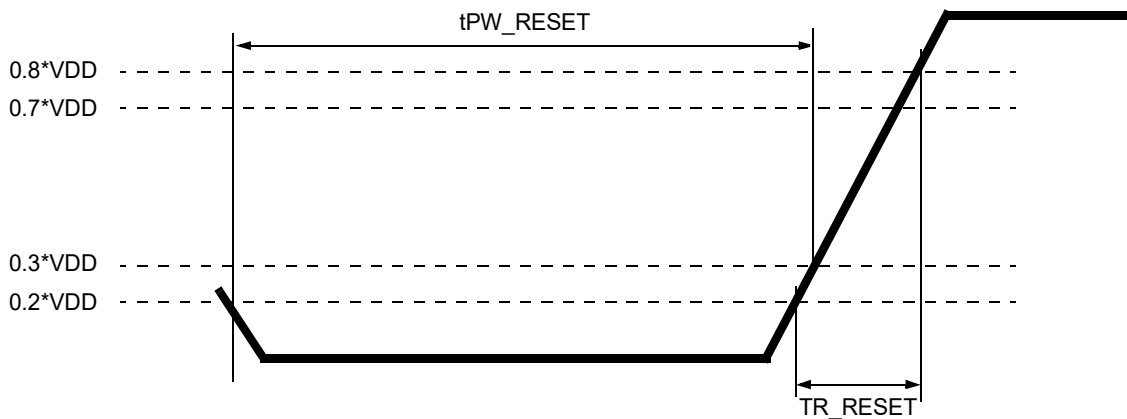
CMOS rail to rail Input Levels for RESET_n

CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
Rising time	TR_RESET	-	1.0	us	4
RESET pulse width	tPW_RESET	1.0	-	us	3,5

NOTE :

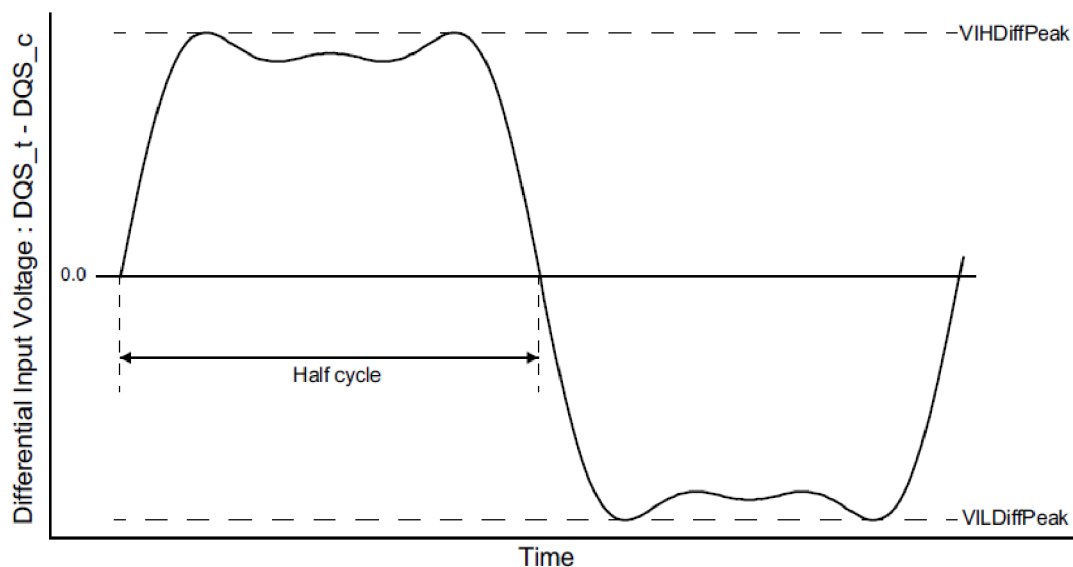
1. After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. No slope reversal(ringback) requirement during its level transition from Low to High.
5. This definition is applied only "Reset Procedure at Power Stable".
6. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings



RESET_n Input Slew Rate Definition

AC and DC Logic Input Levels for DQS Signals

Differential signal definition



Definition of differential DQS Signal AC-swing Level

Differential swing requirements for DQS (DQS_t - DQS_c)

Differential AC and DC Input Levels for DQS

Symbol	Parameter	DDR4-1600,1866,2133		DDR4-2400		DDR4-2666		Unit	Note
		Min	Max	Min	Max	Min	Max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	186	Note2	160	Note2	150	Note2	mV	1
VILDiffPeak	VIL.DIFF.Peak Voltage	Note2	-186	Note2	-160	Note2	-150	mV	1

Symbol	Parameter	DDR4-2933		DDR4-3200		Unit	Note
		Min	Max	Min	Max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	145	Note2	140	Note2	mV	1
VILDiffPeak	VIL.DIFF.Peak Voltage	Note2	-145	Note2	-140	mV	1

NOTE :

- Used to define a differential signal slew-rate.
- These values are not defined; however, the differential signals DQS_t - DQS_c, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

Peak voltage calculation method

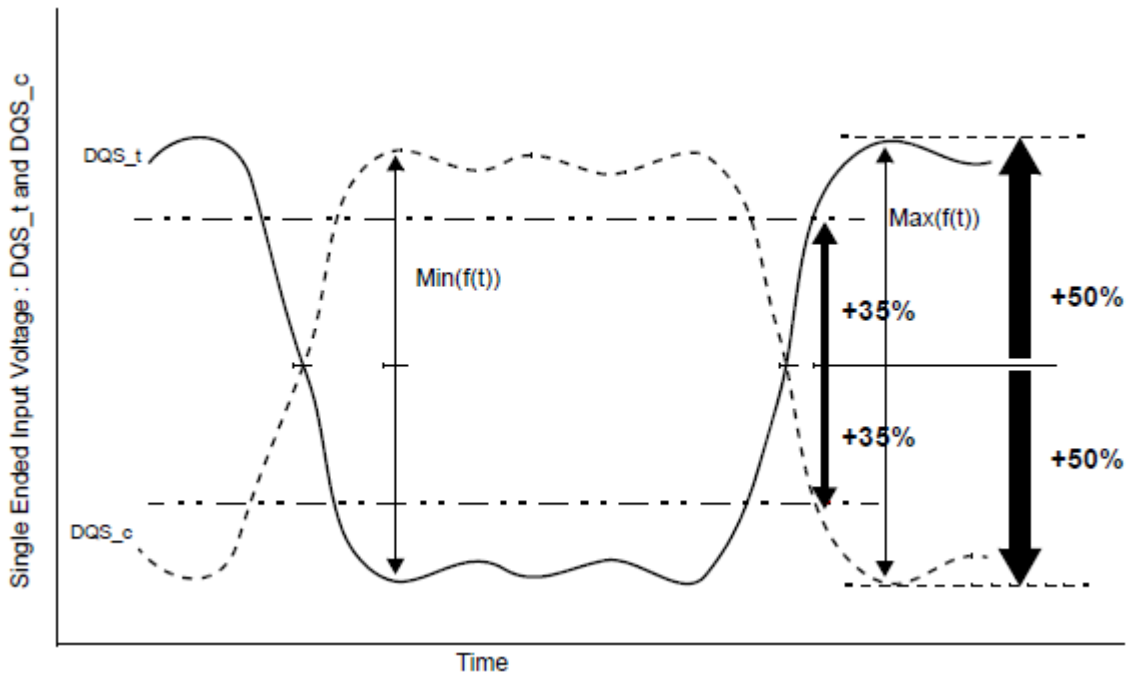
The peak voltage of Differential DQS signals are calculated in a following equation.

$$\mathbf{VIH.DIFF.Peak\ Voltage = Max(f(t))}$$

$$\mathbf{VIL.DIFF.Peak\ Voltage = Min(f(t))}$$

$$\mathbf{f(t) = VDQS_t - VDQS_c}$$

The Max(f(t)) or Min(f(t)) used to determine the midpoint which to reference the +/-35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all ui's.



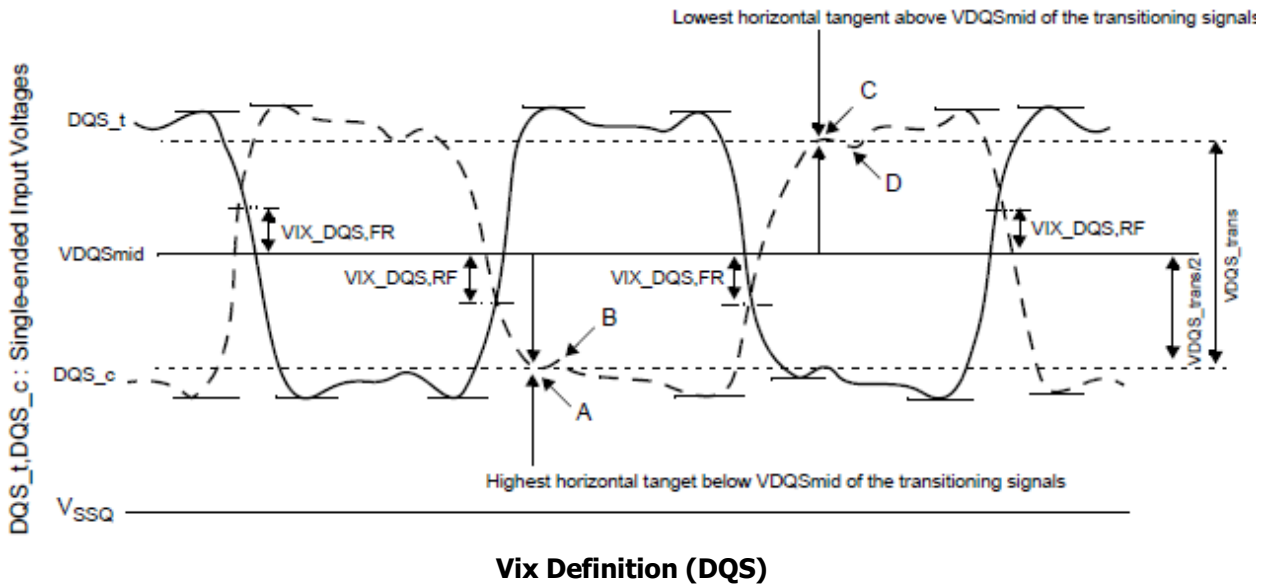
Definition of differential DQS Peak Voltage and range of exempt non-monotonic signaling

Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table below. The differential input cross point voltage VIX_{DQS} (VIX_{DQS_FR} and VIX_{DQS_RF}) is measured from the actual cross point of DQS_t, DQS_c relative to the VDQSmid for the DQS_t and DQS_c signals.

VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by VDQSmid. VDQSmid is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.

A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/- 30% of the midpoint of either VID_{DIFF}.Peak Voltage (DQS_t rising) or VIL_{DIFF}.Peak Voltage (DQS_c rising), refer to Future Definition of differential DQS Peak Voltage and range of exempt non-monotonic signaling. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Figure below) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Figure below) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Figure below) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Figure below) is not a valid horizontal tangent.



Cross point voltage for differential input signals

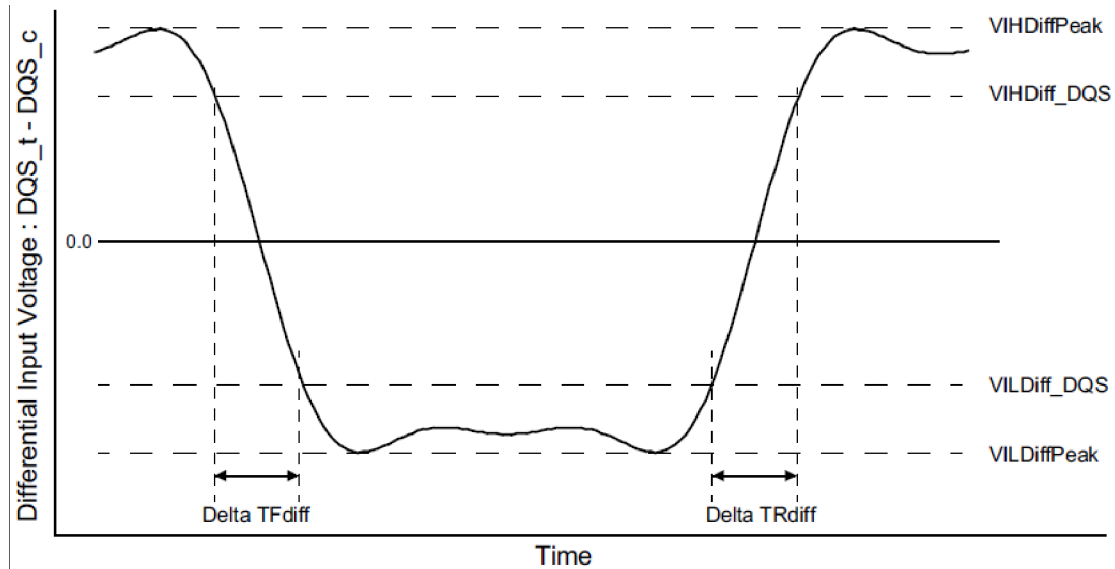
Symbol	Parameter	DDR4-1600,1866,2133,2400		DDR4-2666,2933,3200		Unit	Note
		Min	Max	Min	Max		
Vix_DOS_ratio	DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	-	25	-	25	%	1,2
VDQSmid_to_Vcent	VDQSmid offset relative to Vcent_DQ(midpoint)	-	min(VIH-diff, 50)	-	min(VIH-diff, 50)	mV	3,4,5

NOTE :

1. Vix_DQS_Ratio is DQS VIX crossing (Vix_DQS_FR or Vix_DQS_RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
2. VDQSmid will be similar to the VREFDQ internal setting value obtained during Vref Training if the DQS and DQS drivers and paths are matched.
3. The maximum limite shall not exceed the smaller of VIHdiff minimum limit or 50mV.
4. VIX measurements are only applicable for transitioning DQS_t and DQS_c signals when toggling data, preamble and high-z states are not applicable conditions.
5. The parameter VDQSmid is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure below.



NOTE :

1. Differential signal rising edge from VILDiff_DQS to VIHDiff_DQS must be monotonic slope.
2. Differential signal falling edge from VIHDiff_DQS to VILDiff_DQS must be monotonic slope.

Differential Input Slew Rate Definition for DQS_t, DQS_c

Differential Input Slew Rate Definition for DQS_t, DQS_c

Description			Defined by
	From	To	
Differential input slew rate for rising edge(DQS_t - DQS_c)	VILDiff_DQS	VIHDiff_DQS	$ VILDiff_DQS - VIHDiff_DQS / \Delta TRdiff$
Differential input slew rate for falling edge(DQS_t - DQS_c)	VIHDiff_DQS	VILDiff_DQS	$ VILDiff_DQS - VIHDiff_DQS / \Delta TFdiff$

Differential Input Level for DQS_t, DQS_c

Symbol	Parameter	DDR4-1600,1866,2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
VIHDiff_DQS	Differential Input High	136	-	130	-	130	-	115	-	110	-	mV	
VILDiff_DQS	Differential Input Low	-	-136	-	-130	-	-130	-	-115	-	-110	mV	

Differential Input Slew Rate for DQS_t, DQS_c

Symbol	Parameter	DDR4-1600,1866,2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
SRIdiff	Differential Input Slew Rate	3	18	3	18	2.5	18	2.5	18	2.5	18	V/ns	

AC and DC output Measurement levels

Single-ended AC & DC Output Levels

Single-ended AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/ 2400/2666/3200	Units	NOTE
V _{OH} (DC)	DC output high measurement level (for IV curve linearity)	1.1 × V _{DDQ}	V	
V _{OM} (DC)	DC output mid measurement level (for IV curve linearity)	0.8 × V _{DDQ}	V	
V _{OL} (DC)	DC output low measurement level (for IV curve linearity)	0.5 × V _{DDQ}	V	
V _{OH} (AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) × V _{DDQ}	V	1
V _{OL} (AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) × V _{DDQ}	V	1

NOTE :

1. The swing of $\pm 0.15 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $RZQ/7\Omega$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

Differential AC & DC Output Levels

Differential AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/ 2133/2400/2666/3200	Units	NOTE
V _{OHdiff} (AC)	AC differential output high measurement level (for output SR)	+0.3 × V _{DDQ}	V	1
V _{OLdiff} (AC)	AC differential output low measurement level (for output SR)	-0.3 × V _{DDQ}	V	1

NOTE :

1. The swing of $\pm 0.3 \times V_{DDQ}$ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of $RZQ/7\Omega$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$ at each of the differential outputs.

Single-ended Output Slew Rate

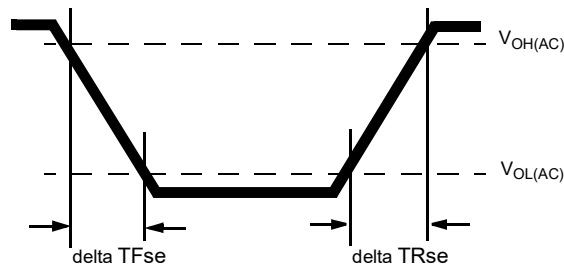
With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table and Figure below.

Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TR_{se}$
Single ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TF_{se}$

NOTE :

1. Output slew rate is verified by design and characterization, and may not be subject to production test.



Single-ended Output Slew Rate Definition

Single-ended output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

NOTE:

1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.

-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

Differential Output Slew Rate

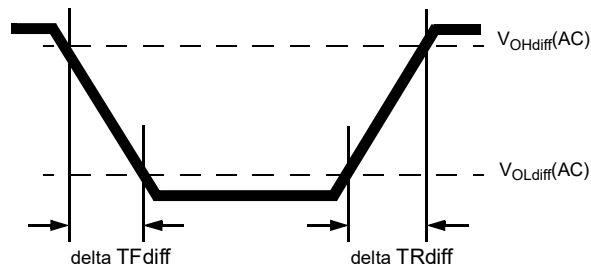
With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff}(AC)$ and $V_{OHdiff}(AC)$ for differential signals as shown in Table and Figure below.

Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)] / \Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)] / \Delta TF_{diff}$

NOTE :

- Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output Slew Rate Definition

Differential output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	8	18	8	18	8	18	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

For Ron = RZQ/7 setting

Single-ended AC & DC Output Levels of Connectivity Test Mode

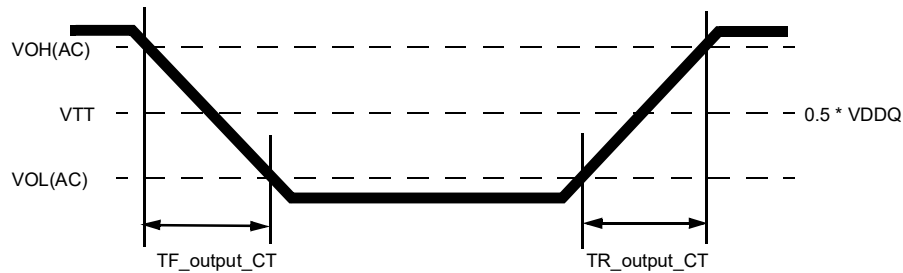
Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

Single-ended AC & DC output levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133/ 2400/2666/3200	Unit	Note
V _{OH} (DC)	DC output high measurement level (for IV curve linearity)	1.1 x V _{DDQ}	V	
V _{OM} (DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V _{DDQ}	V	
V _{OL} (DC)	DC output low measurement level (for IV curve linearity)	0.5 x V _{DDQ}	V	
V _{OB} (DC)	DC output below measurement level (for IV curve linearity)	0.2 x V _{DDQ}	V	
V _{OH} (AC)	AC output high measurement level (for output SR)	V _{TT} + (0.1 x V _{DDQ})	V	1
V _{OL} (AC)	AC output below measurement level (for output SR)	V _{TT} - (0.1 x V _{DDQ})	V	1

NOTE :

1. The effective test load is 50Ω terminated by V_{TT} = 0.5 * V_{DDQ}.



Differential Output Slew Rate Definition of Connectivity Test Mode

Single-ended output slew rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133/2400/2666/3200		Unit	Note
		Min	Max		
Output signal Falling time	TF _{output_CT}	-	10	ns/V	
Output signal Rising time	TR _{output_CT}	-	10	ns/V	

Standard Speed Bins

DDR4-2400 Speed Bins and Operations

Speed Bin		DDR4-2400U-3DS2A		Unit	NOTE
CL-nRCD-nRP		20-18-18			
Parameter	Symbol	min	max		
Internal read command to first data	tAA	16.67	21.5	ns	
ACT to internal read or write delay time	tRCD	15.00	-	ns	
PRE command period	tRP	15.00	-	ns	
ACT to PRE command period	tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00	-		11
CWL = 9,11	CL = 13	tCK(AVG)	Reserved	ns	1,2,3,4,8
	CL = 14	tCK(AVG)	1.25 <1.5	ns	1,2,3,8
CWL = 10,12	CL = 14	tCK(AVG)	Reserved	ns	1,2,3,4,8
	CL = 15	tCK(AVG)	Reserved	ns	1,2,3,4,8
	CL = 16	tCK(AVG)	1.071 <1.25	ns	1,2,3,8
CWL = 11,14	CL = 16	tCK(AVG)	Reserved	ns	1,2,3,4,8
	CL = 18	tCK(AVG)	0.937 <1.071	ns	1,2,3,4,8
	CL = 20	tCK(AVG)	Reserved	ns	1,2,3,4,8
CWL = 12,16	CL = 18	tCK(AVG)	0.937 <1.071	ns	1,2,3,4
	CL = 20	tCK(AVG)	0.833 <0.937	ns	1,2,3,4
	CL = 22	tCK(AVG)	Reserved	ns	1,2,3,4,8
Supported CL Settings		14,16,18,20		nCK	
Supported nRCD Timings minimum		10		nCK	
Supported nRP Timings minimum		10		nCK	
Supported CWL Settings		9,10,11,12,14,16		nCK	

DDR4-2666 Speed Bins and Operations

Speed Bin		DDR4-2666V-3DS3A		Unit	NOTE
CL-nRCD-nRP		22-19-19			
Parameter	Symbol	min	max		
Internal read command to first data	tAA	16.5	21.5	ns	
ACT to internal read or write delay time	tRCD	14.25	-	ns	
PRE command period	tRP	14.25	-	ns	
ACT to PRE command period	tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period	tRC	46.25	-	ns	
CWL = 9,11	CL = 13	tCK(AVG)	Reserved	ns	1,2,3,4,9
	CL = 14	tCK(AVG)	1.25 <1.5	ns	1,2,3,9
CWL = 10,12	CL = 14	tCK(AVG)	Reserved	ns	1,2,3,4,9
	CL = 15	tCK(AVG)	Reserved	ns	1,2,3,4,9
	CL = 16	tCK(AVG)	1.071 <1.25	ns	1,2,3,9
CWL = 11,14	CL = 16	tCK(AVG)	Reserved	ns	1,2,3,4,9
	CL = 18	tCK(AVG)	0.937 <1.071	ns	1,2,3,4,9
	CL = 20	tCK(AVG)	0.937 <1.071	ns	1,2,3,9
CWL = 12,16	CL = 18	tCK(AVG)	Reserved	ns	1,2,3,4,9
	CL = 20	tCK(AVG)	0.833 <0.937	ns	1,2,3,4,9
	CL = 22	tCK(AVG)	0.833 <0.937	ns	1,2,3,9
CWL = 14,18	CL = 20	tCK(AVG)	Reserved	ns	1,2,3,4,9
	CL = 22	tCK(AVG)	0.75 0.833	ns	1,2,3,4,9
	CL = 24	tCK(AVG)	0.75 0.833	ns	1,2,3,9
Supported CL Settings		14,16,18,20,22,24		nCK	
Supported nRCD Timings minimum		12		nCK	
Supported nRP Timings minimum		12		nCK	
Supported CWL Settings		9,10,11,12,14,16,18		nCK	

DDR4-2933 Speed Bins and Operations

Speed Bin		DDR4-2933Y-3DS3A		Unit	NOTE
CL-nRCD-nRP		24-21-21			
Parameter	Symbol	min	max		
Internal read command to first data	tAA	16.37	21.50	ns	
ACT to internal read or write delay time	tRCD	14.32	-	ns	
PRE command period	tRP	14.32	-	ns	
ACT to PRE command period	tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period	tRC	46.32	-	ns	
CWL = 9,11	CL = 13 tCK(AVG)	Reserved		ns	1,2,3,4,14
	CL = 14 tCK(AVG)	1.25	1.5	ns	1,2,3,4,14
CWL = 10,12	CL = 14 tCK(AVG)	Reserved		ns	1,2,3,4,14
	CL = 15 tCK(AVG)	Reserved		ns	1,2,3,4,14
	CL = 16 tCK(AVG)	1.071	<1.25	ns	1,2,3,4,14
CWL = 11,14	CL = 16 tCK(AVG)	Reserved		ns	1,2,3,4,14
	CL = 18 tCK(AVG)	0.937	<1.071	ns	1,2,3,4,14
	CL = 20 tCK(AVG)	0.937	<1.071	ns	1,2,3,4,14
CWL = 12,16	CL = 18 tCK(AVG)	Reserved		ns	1,2,3,4,14
	CL = 20 tCK(AVG)	0.833	<0.937	ns	1,2,3,4,14
	CL = 22 tCK(AVG)	0.833	<0.937	ns	1,2,3,4,14
CWL = 14,18	CL = 20 tCK(AVG)	Reserved		ns	1,2,3,4,14
	CL = 22 tCK(AVG)	0.75	0.833	ns	1,2,3,4,14
	CL = 24 tCK(AVG)	0.75	0.833	ns	1,2,3,4,14
CWL = 16, 20	CL = 22 tCK(AVG)	Reserved		ns	1,2,3,4,14
	CL = 23 tCK(AVG)	Reserved		ns	1,2,3,4,14
	CL = 24 tCK(AVG)	0.682	<0.75	ns	1,2,3,4,14
	CL = 25 tCK(AVG)	0.682	<0.75	ns	1,2,3,4,14
Supported CL Settings		14,16,18,20,22,24,25		nCK	
Supported nRCD Timings minimum		10		nCK	
Supported nRP Timings minimum		10		nCK	
Supported CWL Settings		9,10,11,12,14,16,18,20		nCK	

DDR4-3200 Speed Bins and Operations

Speed Bin		DDR4-3200AA-3DS4A		Unit	NOTE
CL-nRCD-nRP		26-22-22			
Parameter	Symbol	min	max		
Internal read command to first data	tAA	16.25	21.50	ns	
ACT to internal read or write delay time	tRCD	13.75	-	ns	
PRE command period	tRP	13.75	-	ns	
ACT to PRE command period	tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period	tRC	45.75	-	ns	
CWL = 9,11	CL = 13 tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 14 tCK(AVG)	1.25	1.5	ns	1,2,3,10
CWL = 10,12	CL = 14 tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 15 tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 16 tCK(AVG)	1.071	<1.25	ns	1,2,3,10
CWL = 11,14	CL = 16 tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 18 tCK(AVG)	0.937	<1.071	ns	1,2,3,4,10
	CL = 20 tCK(AVG)	0.937	<1.071	ns	1,2,3,10
CWL = 12,16	CL = 18 tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 20 tCK(AVG)	0.833	<0.937	ns	1,2,3,4,10
	CL = 22 tCK(AVG)	0.833	<0.937	ns	1,2,3,10
CWL = 14,18	CL = 20 tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 22 tCK(AVG)	0.75	0.833	ns	1,2,3,4,10
	CL = 24 tCK(AVG)	0.75	0.833	ns	1,2,3,10
CWL = 16, 20	CL = 22 tCK(AVG)	Reserved		ns	1,2,3,10
	CL = 24 tCK(AVG)	0.625	<0.75	ns	1,2,3,10
	CL = 25 tCK(AVG)	0.625	<0.75	ns	1,2,3,10
Supported CL Settings		14,16,18,20,22,24,26,28		nCK	
Supported nRCD Timings minimum		12		nCK	
Supported nRP Timings minimum		11		nCK	
Supported CWL Settings		9,10,11,12,14,16,18,20		nCK	

Speed Bin Table Notes

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133, 2400 Speed Bin Tables are valid only when Gear Down Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following the rounding algorithm defined in JESD79-4.
3. tCK(avg).MAX limits: Calculate $tCK(avg) = tAA.MAX / CL\ SELECTED$ and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Any combination of the 'optional' CL's is supported. The associated 'optional' tAA, tRCD, tRP, and tRC values must be adjusted based upon the CL combination supported. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-3DS-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-3DS-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-3DS-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-3DS-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Any DDR4-3DS-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
11. Any DDR4-3DS-2933 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
12. CL number in parenthesis, it means that these numbers are optional.
13. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.
14. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as started in the Speed Bin Tables.
15. DDR4 SDRAM supports CL=20 as long as a system meets tAA(min), tRCD(min), tRP(min), and tRC(min)
16. DDR4-2400U-3DS2A CL-nRCD-nRP=20-18-18 timing will change to 20-17-17 if the 'optional' CL18 setting is supported.

Refresh Command

No more than one logical rank Refresh Command can be initiated simultaneously to DDR4 3D Stacked SDRAMs as shown in Table below.

The minimum refresh cycle time to a single logical rank (=tRFC_slr) has the same value as tRFC for a planar DDR4 SDRAM of the same density as the logical rank.

The minimum time between issuing refresh commands to different logical ranks is specified as tRFC_dlr. After a Refresh command to a logical rank, other valid commands can be issued before tRFC_dlr to the other logical ranks that are not the target of the refresh.

Truth Table for Refresh Command

DRAM Command	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	Note5
Refresh (REF)	L	L	L	L	REF	DES	DES	DES	DES	DES	DES	DES	1
Refresh (REF)	L	L	L	H	DES	REF	DES	DES	DES	DES	DES	DES	1
Refresh (REF)	L	L	H	L	DES	DES	REF	DES	DES	DES	DES	DES	1
Refresh (REF)	L	L	H	H	DES	DES	DES	REF	DES	DES	DES	DES	1
Refresh (REF)	L	H	L	L	DES	DES	DES	DES	REF	DES	DES	DES	1
Refresh (REF)	L	H	L	H	DES	DES	DES	DES	DES	REF	DES	DES	1
Refresh (REF)	L	H	H	L	DES	DES	DES	DES	DES	DES	REF	DES	1
Refresh (REF)	L	H	H	H	DES	DES	DES	DES	DES	DES	DES	REF	1
Any command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	1, 2

NOTE 1 CKE=H.

NOTE 2 "V" means H or L (but a defined logic level).

In general, a Refresh command needs to be issued to each logical rank in 3D Stacked DDR4 SDRAM regularly every tREFI_slr interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. For the 8Gb and below density die, a maximum of 8 Refresh commands per logical rank can be postponed during operation of the 3D stacked DDR4 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed per logical rank. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to $9 \times tREFI_slr$. A maximum of 8 additional Refresh commands can be issued in advance ("pulled in") per logical rank, with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum

interval between two surrounding Refresh commands is limited to $9 \times tREFI_slr$. At any given time, a maximum of 16 REF commands per logical rank can be issued within $2 \times tREFI_slr$. Self-Refresh Mode may be entered with a maximum of eight Refresh commands per logical rank being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight per logical rank.

For the 16Gb and above density die, the number of burst refresh commands per 3D Stacked DDR4

Package is limited to a maximum of 16 to prevent power drop. That is no more than a total of 16 Refresh commands are allowed to be issued in 3.9us for FGR1 mode, 1.95us for FGR2 mode, 0.975us for FGR4 mode per 3D Stacked DDR4 package. In case that 16 Refresh commands are postponed in a row for 3D stacked DDR4 package, the resulting maximum interval between the surrounding Refresh commands is limited to $9 \times t_{REFI_slr}$ for 2H 3D Stacked DDR4 SDRAM, $5 \times t_{REFI_slr}$ for 4H 3D Stacked DDR4 SDRAM. A maximum of 16 additional Refresh commands can be issued in advance("pulled in") per 3D Stacked DDR4 package, with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 16 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to $9 \times t_{REFI_slr}$ for 2H 3D Stacked DDR4 SDRAM and $5 \times t_{REFI_slr}$ for 4H 3D Stacked DDR4 SDRAM. At any given time, a maximum of 16 Refresh commands per 3D Stacked DDR4 package can be issued within 3.9us for FGR1 mode, 1.95us for FGR2 mode, 0.975us for FGR4 mode. Self-Refresh Mode may be entered with a maximum of 16 Refresh commands per 3D Stacked DDR4 package being postponed. After exiting Self-Refresh Mode with one or more Refresh commands, additional Refresh commands may be postponed to the extent that total number of postponed Refresh commands(before and after the Self-Refresh) will never exceed 16 per 3D Stacked DDR4 package. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

Refresh parameters

Typical platforms are designed with the assumption that no more than one physical rank is refreshed at the same time. In order to limit the maximum refresh current (IDD5B1) for a 3D stacked SDRAM, it will be required to stagger the refreshes to each device in a stack.

The tRFC time for a single logical rank is defined as tRFC_slr and is specified as the same value as for a monolithic DDR4 SDRAM of equivalent density. The minimum amount of stagger between refresh commands (=tREF_stagger) sent to different logical ranks is specified to be approximately tRFC_slr/3 -as shown in Table below.

Refresh parameters by logical rank density

Parameter	Symbol		Logical Rank Density		Unit	Note
			16Gb			
			Default	Optional		
REF command to ACT or REF command time to same logical rank	tRFC_slr1 (1x mode)		550	350	ns	
	tRFC_slr2 (2x mode)		350	260	ns	
	tRFC_slr4 (4x mode)		260	160	ns	
REF command to REF command to different logical rank	tRFC_dlr1 (1x mode)		190	120	ns	
	tRFC_dlr2 (2x mode)		120	90	ns	
	tRFC_dlr4 (4x mode)		90	55	ns	
Average periodic refresh interval in same logical rank	tREFI_slr1 (1x mode)	0 °C =< T _{CASE} =< 85 °C	7.8		us	
		85 °C < T _{CASE} =< 95 °C	3.9		us	
	tREFI_slr2 (2x mode)	0 °C =< T _{CASE} =< 85 °C	3.9		us	
		85 °C < T _{CASE} =< 95 °C	1.95		us	
	tREFI_slr4 (4x mode)	0 °C =< T _{CASE} =< 85 °C	1.95		us	
		85 °C < T _{CASE} =< 95 °C	0.975		us	

IDD and IDDQ Specification Parameters and Test Conditions

IDD, IPP and IDDQ Measurement Conditions

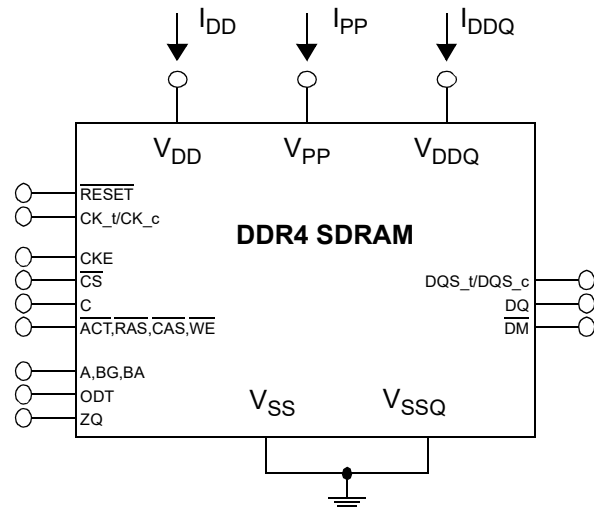
In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD5B1, IDD5B2, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In SDRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as $V_{IN} \leq V_{ILAC}(\max)$.
- "1" and "HIGH" is defined as $V_{IN} \geq V_{IHAC}(\min)$.
- "MID-LEVEL" is defined as inputs are $V_{REF} = V_{DD} / 2$.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 11.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
 - RON = RZQ/7 (34 Ohm in MR1);
 - RTT_NOM = RZQ/6 (40 Ohm in MR1);
 - RTT_WR = RZQ/2 (120 Ohm in MR2);
 - RTT_PARK = Disable;
 - Qoff = 0_B (Output Buffer enabled) in MR1;
 - TDQS_t Feature disabled in MR1;
 - CRC disabled in MR2;
 - CA parity feature disabled in MR5;
 - Gear Down mode disabled in MR3
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD, IPP or IDDQ measurement is started.
- Define D = {CS0_n, ACT_n, RAS_n, CAS_n, WE_n} := {HIGH, LOW, LOW, LOW, LOW}
- Define D# = {CS0_n, ACT_n, RAS_n, CAS_n, WE_n} := {HIGH, HIGH, HIGH, HIGH, HIGH}



NOTE:

1. DIMM level Output test load condition may be different from above

Figure 1 - Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

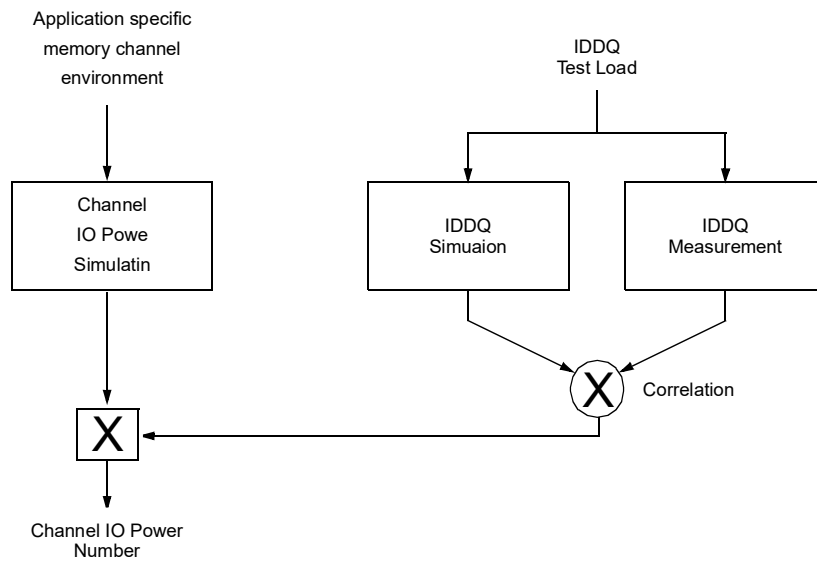


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol	DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit
	20-18-18		22-19-19		24-21-21		26-22-22		
tCK	0.833		0.75		0.682		0.625		ns
CL	20		22		24		26		nCK
CWL	16		18		20		20		nCK
nRCD	18		19		21		22		nCK
nRC	57		62		68		74		nCK
nRAS	39		43		47		52		nCK
nRP	18		19		21		22		nCK
nFAW_slr	x4	16	16	16	16	16	16	nCK	
nRRD_S_slr	x4	4	4	4	4	4	4	nCK	
nRRD_L_slr	x4	6	7	8	8	8	8	nCK	
nRFC_slr	4Gb	313	347	382	416	nCK			
nRFC_slr	8Gb	421	467	514	560	nCK			
nRFC_slr	16Gb	661	734	807	880	nCK			
nRFC_dlr	4Gb	109	120	132	144	nCK			
nRFC_dlr	8Gb	145	160	176	192	nCK			
nRFC_dr	16Gb	229	254	279	304	nCK			

Table 2 -Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 3; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3); Logical Rank Activity: Cycling with one logical rank active at a time; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 3
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-2) AL = CL-2, Other conditions: see IDD0
IPP0	Operating One Bank Active-Precharge IPP Current Same condition with IDD0
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling according to Table 4; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 4); Logical Rank Activity: Cycling with one logical rank active at a time; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 4
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-2) AL = CL-2, Other conditions: see IDD1
IPP1	Operating One Bank Active-Read-Precharge IPP Current Same condition with IDD1
IDD2N	Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 5
IDD2NA	Precharge Standby Current (AL=CL-2) AL = CL-2, Other conditions: see IDD2N
IPP2N	Precharge Standby IPP Current Same condition with IDD2N
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 6; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: toggling according to Table 6; Pattern Details: see Table 6
IDDQ2NT (Optional)	Precharge Standby ODT IDDQ Current Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled ³
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled ³

IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled ³
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled ³
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0
IPP2P	Precharge Power-Down IPP Current Same condition with IDD2P
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 5
IDD3NA	Active Standby Current (AL=CL-2) AL = CL-2, Other conditions: see IDD3N
IPP3N	Active Standby IPP Current Same condition with IDD3N
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0
IPP3P	Active Power-Down IPP Current Same condition with IDD3P
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ² ; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM_n: stable at 1; Bank Activity: all banks of all logical ranks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 7) and through logical ranks; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 7
IDD4RA	Operating Burst Read Current (AL=CL-2) AL = CL-2, Other conditions: see IDD4R
IPP4R	Operating Burst Read IPP Current Same condition with IDD4R
IDDQ4R (Optional)	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current

IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless write data burst with different data between one burst and the next one according to Table 8; DM_n: stable at 1; Bank Activity: all banks open of all logical ranks, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 8) and through logical ranks; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at HIGH; Pattern Details: see Table 8
IDD4WA	Operating Burst Write Current (AL=CL-2) AL = CL-2, Other conditions: see IDD4W
IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled ³ , Other conditions: see IDD4W
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled ³ , Other conditions: see IDD4W
IPP4W	Operating Burst Write IPP Current Same condition with IDD4W
IDD5B1	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC (see Table 9); Logical Rank Activity: REF command staggered nRFC_dlr between REF command to REF command; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 9
IPP5B1	Burst Refresh Write IPP Current (1X REF) Same condition with IDD5B1
IDD5B2	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC (see Table 9); Logical Rank Activity: REF command staggered nRFC_slr between REF command to REF command; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 9
IPP5B2	Burst Refresh Write IPP Current (1X REF) Same condition with IDD5B2
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B2
IPP5F2	Burst Refresh Write IPP Current (2X REF) Same condition with IDD5F2
IPP5F3	Burst Refresh Write IPP Current (2X REF) Same condition with IDD5F3
IDD5F3	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B1
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B1
IPP5F4	Burst Refresh Write IPP Current (4X REF) Same condition with IDD5F4
IDD5F5	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B2

IPP5F5	Burst Refresh Write IPP Current (4X REF) Same condition with IDD5F5
IDD6N	Self Refresh Current: Normal Temperature Range T_{CASE} : 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal ⁴ ; CKE : Low; External clock : Off; CK_t and CK_c : LOW; CL : see Table 1; BL : 8 ¹ ; AL : 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO : High; DM_n : stable at 1; Bank Activity : Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL
IPP6N	Self Refresh IPP Current: Normal Temperature Range Same condition with IDD6N
IDD6E	Self-Refresh Current: Extended Temperature Range T_{CASE} : 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended ⁴ ; CKE : Low; External clock : Off; CK_t and CK_c : LOW; CL : see Table 1; BL : 8 ¹ ; AL : 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO : High; DM_n :stable at 1; Bank Activity : Extended Temperature Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL
IPP6E	Self Refresh IPP Current: Extended Temperature Range Same condition with IDD6E
IDD6R	Self-Refresh Current: Reduced Temperature Range T_{CASE} : 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced ⁴ ; CKE : Low; External clock : Off; CK_t and CK_c : LOW; CL : see Table 1; BL : 8 ¹ ; AL : 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO : High; DM_n :stable at 1; Bank Activity : Extended Temperature Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL
IPP6R	Self Refresh IPP Current: Reduced Temperature Range Same condition with IDD6R
IDD6A	Auto Self-Refresh Current T_{CASE} : 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto ⁴ ; Partial Array Self-Refresh (PASR) : Full Array; CKE : Low; External clock : Off; CK_t and CK_c : LOW; CL : see Table 1; BL : 8 ¹ ; AL : 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO : High; DM_n :stable at 1; Bank Activity : Auto Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL
IPP6A	Auto Self-Refresh IPP Current Same condition with IDD6A
IDD7	Operating Bank Interleave Read Current CKE : High; External clock : On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL : see Table 1; BL : 8 ¹ ; AL : CL-2; CS_n : High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs : partially toggling according to Table 10; Data IO : read data bursts with different data between one burst and the next one according to Table 10; DM_n : stable at 1; Bank Activity : two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 10; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : stable at 0; Pattern Details : see Table 10
IPP7	Operating Bank Interleave Read IPP Current Same condition with IDD7
IDD8	Maximum Power Down Current TBD
IPP8	Maximum Power Down IPP Current Same condition with IDD8

NOTE :

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable
 - set MR1 [A12 = 0] : Qoff = Output buffer enabled
 - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
 - RTT_Nom enable
 - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6
 - RTT_WR enable
 - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2
 - RTT_PARK disable
 - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
010] : 1866MT/s, 2133MT/s
011] : 2400MT/s
 - Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate
 - DLL disabled : set MR1 [A0 = 0]
 - CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
010] : 2400MT/s
 - Read DBI enabled : set MR5 [A12 = 1]
 - Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
 - 01] : Reduced Temperature range
 - 10] : Extended Temperature range
 - 11] : Auto Self Refresh
5. IDD2NG should be measured after sync pulse(NOP) input.

Table 3 - IDD0, IDD0A and IPP0 Measurement-Loop Pattern¹

CK_t / CK_c	CKE	Sub-Loop	Logical Rank -Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n / A16	CAS_n / A15	WE_n / A14	ODT	C[2:0] ²	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³				
toggling	Static High	0	0	0	ACT	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	-				
				1,2	D, D	1	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	-		
				3,4	D_#, D_#	1	1	1	1	1	1	0	000	3	3	0	0	0	7	F	0	0	-		
				...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																				
				nRAS	PRE	0	1	0	1	0	0	0	000	0	0	0	0	0	0	0	0	0	0	-	
				...	repeat pattern 1...4 until nRC - 1, truncate if necessary																				
				1	1*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 001 instead																			
				2	2*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 010 instead																			
		3	3*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 011 instead																					
		4	4*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 100 instead																					
		5	5*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 101 instead																					
		6	6*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 110 instead																					
		7	7*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 111 instead																					
		1	8*nRC	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 1 instead																					
		2	16*nRC	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead																					
		3	24*nRC	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 3 instead																					
		4	32*nRC	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead																					
		5	40*nRC	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 2 instead																					
		6	48*nRC	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead																					
		7	56*nRC	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 0 instead																					
8	64*nRC	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 0 instead																							
9	72*nRC	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 1 instead																							
10	80*nRC	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 2 instead																							
11	88*nRC	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 3 instead																							
12	96*nRC	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 1 instead																							
13	104*nRC	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 2 instead																							
14	112*nRC	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 3 instead																							
15	120*nRC	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 0 instead																							

NOTE:

1. DQS_t, DQS_c are VDDQ.
2. C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
3. DQ signals are VDDQ.

Table 4 - IDD1, IDD1A and IPP1 Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Logical Rank -Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ²	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³					
toggling	Static High	0	0	0	ACT	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	-				
				1, 2	D, D	1	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	0	-		
				3, 4	D#, D#	1	1	1	1	1	1	0	000	3	3	0	0	0	0	7	F	0	0	-		
				...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																					
				nRCD -AL	RD	0	1	1	0	1	0	000	0	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
				...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																					
				nRAS	PRE	0	1	0	1	0	0	000	0	0	0	0	0	0	0	0	0	0	0	0	-	
				...	repeat pattern 1...4 until nRC - 1, truncate if necessary																					
				1	1*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 001 instead																				
				2	2*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 010 instead																				
				3	3*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 011 instead																				
				4	4*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 100 instead																				
				5	5*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 101 instead																				
				6	6*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 110 instead																				
				7	7*nRC	repeat Logical Rank-loop 0, use C[2:0] ² = 111 instead																				
				1	0	8*nRC + 0	0	ACT	0	0	0	1	1	0	000	1	1	0	0	0	0	0	0	0	0	-
		8*nRC + 1, 2	D, D				1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	0	0	-	
		8*nRC + 3, 4	D#, D#				1	1	1	1	1	0	000	3 ^b	3	0	0	0	0	7	F	0	0	0	-	
		...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																							
		8*nRC + nRCD - AL	RD				0	1	1	0	1	0	000	1	1	0	0	0	0	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
		...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																							
		8*nRC + nRAS	PRE				0	1	0	1	0	0	000	0	0	0	0	0	0	0	0	0	0	0	0	-
		...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																							
		1	9*nRC				repeat Logical Rank-loop 0, use C[2:0] ² = 001 instead																			
		2	10*nRC				repeat Logical Rank-loop 0, use C[2:0] ² = 010 instead																			
		3	11*nRC				repeat Logical Rank-loop 0, use C[2:0] ² = 011 instead																			
		4	12*nRC				repeat Logical Rank-loop 0, use C[2:0] ² = 100 instead																			
		5	13*nRC				repeat Logical Rank-loop 0, use C[2:0] ² = 101 instead																			
		6	14*nRC				repeat Logical Rank-loop 0, use C[2:0] ² = 110 instead																			
		7	15*nRC				repeat Logical Rank-loop 0, use C[2:0] ² = 111 instead																			
		2	16*nRC				repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead																			

CK_t, CK_c	CKE	Sub-Loop Logical Rank -Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ²	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³		
toggling	Static High	3	24*nRC	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 3 instead																		
		4	32*nRC	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead																		
		5	40*nRC	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead																		
		6	48*nRC	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead																		
		7	56*nRC	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead																		
		8	64*nRC	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead																		
		9	72*nRC	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 1 instead																		
		10	80*nRC	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 2 instead																		
		11	88*nRC	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 3 instead																		
		12	96*nRC	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 1 instead																		
		13	104*nRC	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 2 instead																		
		14	112*nRC	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 3 instead																		
		15	120*nRC	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 0 instead																		

NOTE:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
3. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

Table 5 - IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ²	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³			
toggling	Static High	0	0	D, D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	0		
		1	1	D, D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	0	0	
		2	2	D#, D#	1	1	1	1	1	1	0	000	3	3	0	0	0	0	7	F	0	0	0
		3	3	D#, D#	1	1	1	1	1	1	0	000	3	3	0	0	0	0	7	F	0	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 1 instead																			
		2	8-11	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead																			
		3	12-15	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 3 instead																			
		4	16-19	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead																			
		5	20-23	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 2 instead																			
		6	24-27	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead																			
		7	28-31	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 0 instead																			
		8	32-35	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 0 instead																			
		9	36-39	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 1 instead																			
		10	40-43	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 2 instead																			
		11	44-47	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 3 instead																			
12	48-51	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 1 instead																					
13	52-55	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 2 instead																					
14	56-59	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 3 instead																					
15	60-63	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 0 instead																					

NOTE :

1. DQS_t, DQS_c are VDDQ.

2. C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.

3. DQ signals are VDDQ.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ²	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³			
toggling	Static High	0	0	D, D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	-		
		1	1	D, D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	0	-	
		2	2	D#, D#	1	1	1	1	1	1	0	000	3	3	0	0	0	0	7	F	0	0	-
		3	3	D#, D#	1	1	1	1	1	1	0	000	3	3	0	0	0	0	7	F	0	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 1 instead																			
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 2 instead																			
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 3 instead																			
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 1 instead																			
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 2 instead																			
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 3 instead																			
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 0 instead																			
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 0 instead																			
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 1 instead																			
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 2 instead																			
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 3 instead																			
12	48-51	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 1 instead																					
13	52-55	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 2 instead																					
14	56-59	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 3 instead																					
15	60-63	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 0 instead																					

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
3. DQ signals are VDDQ.

Table 7 - IDD4R, IDDR4RA and IDDQ4R Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ²	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³			
toggling	Static High	0	0	0	RD	0	1	1	0	1	0	000	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF		
				1	D	1	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	0	-
		2,3	D#, D#	1	1	1	1	1	1	1	0	000	3	3	0	0	0	0	7	F	F	0	-	
		1	1	4	RD	0	1	1	0	1	0	0	000	1	1	0	0	0	0	7	F	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
				5	D	1	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	0	0
		6,7	D#, D#	1	1	1	1	1	1	1	0	000	3	3	0	0	0	0	0	7	F	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead																				
		3	12-15	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 3 instead																				
		4	16-19	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead																				
		5	20-23	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead																				
		6	24-27	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead																				
		7	28-31	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead																				
		8	32-35	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 0 instead																				
		9	36-39	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 1 instead																				
		10	40-43	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 2 instead																				
		11	44-47	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 3 instead																				
		12	48-51	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 1 instead																				
		13	52-55	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 2 instead																				
		14	56-59	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 3 instead																				
		15	60-63	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 0 instead																				
			1	64-127	repeat Logical Rank-loop 0, use C[2:0] ² = 001 instead																			
			2	128-191	repeat Logical Rank-loop 0, use C[2:0] ² = 010 instead																			
			3	192-255	repeat Logical Rank-loop 0, use C[2:0] ² = 011 instead																			
			4	256-319	repeat Logical Rank-loop 0, use C[2:0] ² = 100 instead																			
			5	320-383	repeat Logical Rank-loop 0, use C[2:0] ² = 101 instead																			
			6	384-447	repeat Logical Rank-loop 0, use C[2:0] ² = 110 instead																			
			7	448-511	repeat Logical Rank-loop 0, use C[2:0] ² = 111 instead																			

NOTE :

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
3. Burst Sequence driven on each DQ signal by Read Command.

Table 8 - IDD4W, IDD4WA and IDD4W_par Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ²	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³			
toggling	Static High	0	0	0	WR	0	1	1	0	1	0	000	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF		
				1	D	1	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	0	-
		2,3	D#, D#	1	1	1	1	1	1	1	1	0	000	3	3	0	0	0	0	7	F	0	-	
		1	1	4	4	WR	0	1	1	0	1	0	000	1	1	0	0	0	0	7	F	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
					5	D	1	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	0
		6,7	D#, D#	1	1	1	1	1	1	1	1	0	000	3	3	0	0	0	0	7	F	0	-	
		2	8-11	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead																				
		3	12-15	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 3 instead																				
		4	16-19	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead																				
		5	20-23	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead																				
		6	24-27	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead																				
		7	28-31	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead																				
		8	32-35	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 0 instead																				
		9	36-39	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 1 instead																				
		10	40-43	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 2 instead																				
		11	44-47	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 3 instead																				
		12	48-51	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 1 instead																				
		13	52-55	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 2 instead																				
		14	56-59	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 3 instead																				
		15	60-63	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 0 instead																				
			1	64-127	repeat Logical Rank-loop 0, use C[2:0] ² = 001 instead																			
			2	128-191	repeat Logical Rank-loop 0, use C[2:0] ² = 010 instead																			
			3	192-255	repeat Logical Rank-loop 0, use C[2:0] ² = 011 instead																			
			4	256-319	repeat Logical Rank-loop 0, use C[2:0] ² = 100 instead																			
			5	320-383	repeat Logical Rank-loop 0, use C[2:0] ² = 101 instead																			
			6	384-447	repeat Logical Rank-loop 0, use C[2:0] ² = 110 instead																			
			7	448-511	repeat Logical Rank-loop 0, use C[2:0] ² = 111 instead																			

NOTE :

1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2. C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
3. Burst Sequence driven on each DQ signal by Write Command.

Table 9 - IDD4WC Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ²	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³		
toggling	Static High	0	0	WR	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC	
		1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		3,4	D#, D#	1	1	1	1	1	1	0	0	3	3	0	0	0	0	7	F	0	-	
		5	WR	0	1	1	0	1	0	0	0	1	1	0	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC	
		6,7	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		8,9	D#, D#	1	1	1	1	1	1	0	0	3	3	0	0	0	0	7	F	0	-	
		2	10-14	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead																		
		3	15-19	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 3 instead																		
		4	20-24	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead																		
		5	25-29	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead																		
		6	30-34	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead																		
		7	35-39	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead																		
		8	40-44	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 0 instead																		
		9	45-49	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 1 instead																		
		10	50-54	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead																		
		11	55-59	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 3 instead																		
12	60-64	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 1 instead																				
13	65-69	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 2 instead																				
14	70-74	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 3 instead																				
15	75-79	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 0 instead																				

NOTE :

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
3. Burst Sequence driven on each DQ signal by Write Command.

Table 10 - IDD5B1 Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ²	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³				
toggling	Static High	0	0	0	REF	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	-			
				1	D	1	0	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	-	
		1	0	2	D	1	0	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	-	
				3	D#, D#	1	1	1	1	1	1	0	0	000	3	3	0	0	0	0	7	F	0	-	
				4	D#, D#	1	1	1	1	1	1	0	0	000	3	3	0	0	0	0	7	F	0	-	
				4-7	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 1 instead																				
				8-11	repeat pattern 1...4, use BG[1:0] = 0, BA[1:0] = 2 instead																				
				12-15	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 3 instead																				
				16-19	repeat pattern 1...4, use BG[1:0] = 0, BA[1:0] = 1 instead																				
				20-23	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 2 instead																				
				24-27	repeat pattern 1...4, use BG[1:0] = 0, BA[1:0] = 3 instead																				
				28-31	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 0 instead																				
				32-35	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 0 instead																				
				36-39	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 1 instead																				
				40-43	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 2 instead																				
				44-47	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 3 instead																				
				48-51	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 1 instead																				
				52-55	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 2 instead																				
				56-59	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 3 instead																				
				60-63	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 0 instead																				
				2	1	2	64 ... nRFC_dlr - 1	repeat Sub-Loop 1, until nRFC_dlr - 1, Truncate, if necessary																	
							nRFC_dlr... 2*nRF-C_dlr - 1	repeat Logical Rank-loop 0, use C[2:0] ² = 001 instead																	
		2RFC_dlr... 3*nRF-C_dlr - 1	repeat Logical Rank-loop 0, use C[2:0] ² = 010 instead																						
		3RFC_dlr... 4*nRF-C_dlr - 1	repeat Logical Rank-loop 0, use C[2:0] ² = 011 instead																						
		4RFC_dlr... 5*nRF-C_dlr - 1	repeat Logical Rank-loop 0, use C[2:0] ² = 100 instead																						
		5RFC_dlr... 6*nRF-C_dlr - 1	repeat Logical Rank-loop 0, use C[2:0] ² = 101 instead																						
		6RFC_dlr... 7*nRF-C_dlr - 1	repeat Logical Rank-loop 0, use C[2:0] ² = 110 instead																						
		7RFC_dlr... 8*nRF-C_dlr - 1	repeat Logical Rank-loop 0, use C[2:0] ² = 111 instead																						

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
3. DQ signals are VDDQ.

Table 11 - IDD5B2 Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ²	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³						
toggling	Static High	0	0	0	REF	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	-					
				1	D	1	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	0	-			
						2	D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	0	-			
						3	D#, D#	1	1	1	1	1	0	000	3	3	0	0	0	0	7	F	0	0	-		
						4	D#, D#	1	1	1	1	1	0	000	3	3	0	0	0	0	7	F	0	0	-		
						4-7	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 1 instead																				
						8-11	repeat pattern 1...4, use BG[1:0] = 0, BA[1:0] = 2 instead																				
						12-15	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 3 instead																				
						16-19	repeat pattern 1...4, use BG[1:0] = 0, BA[1:0] = 1 instead																				
						20-23	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 2 instead																				
						24-27	repeat pattern 1...4, use BG[1:0] = 0, BA[1:0] = 3 instead																				
						28-31	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 0 instead																				
						32-35	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 0 instead																				
						36-39	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 1 instead																				
						40-43	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 2 instead																				
						44-47	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 3 instead																				
						48-51	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 1 instead																				
						52-55	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 2 instead																				
						56-59	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 3 instead																				
						60-63	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 0 instead																				
						2		64 ... nRFC_slr - 1	repeat Sub-Loop 1, until nRFC_slr - 1, Truncate, if necessary																		
								1	nRFC_slr... 2*nRF-C_slr - 1	repeat Logical Rank-loop 0																	
				2	2RFC_slr... 3*nRF-C_slr - 1	repeat Logical Rank-loop 0																					
				3	3RFC_slr... 4*nRF-C_slr - 1	repeat Logical Rank-loop 0																					
				4	4RFC_slr... 5*nRF-C_slr - 1	repeat Logical Rank-loop 0																					
				5	5RFC_slr... 6*nRF-C_slr - 1	repeat Logical Rank-loop 0																					
				6	6RFC_slr... 7*nRF-C_slr - 1	repeat Logical Rank-loop 0																					
				7	7RFC_slr... 8*nRF-C_slr - 1	repeat Logical Rank-loop 0																					

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
3. DQ signals are VDDQ.

Table 12 - IDD7 Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ²	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³				
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-			
			1	RDA	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF		
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3	D#	1	1	1	1	1	1	0	0	0	3 ²	3	0	0	0	0	7	F	0	-	
			...	repeat pattern 2...3 until nRRD - 1, if nRCD > 4. Truncate if necessary																				
			1	nRRD	ACT	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	-
			nRRD + 1	RDA	0	1	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRCD > 4. Truncate if necessary																				
			2	2*nRRD	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead																			
			3	3*nRRD	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 3 instead																			
			4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if necessary																			
			5	nFAW	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead																			
			6	nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead																			
			7	nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead																			
			8	nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead																			
			9	nFAW + 4*nRRD	repeat Sub-Loop 4																			
			10	2*nFAW	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 0 instead																			
			11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 1 instead																			
			12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 2 instead																			
			13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 3 instead																			
14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																						
15	3*nFAW	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 1 instead																						
16	3*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 2 instead																						
17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 3 instead																						
18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 0 instead																						
19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																						
20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																						

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
3. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

IDD Specifications

Module IDD values in the datasheet are only a calculation based on the component IDD spec and register power. The actual measurements may vary according to DQ loading cap.

256GB, 32Gx 72 R-DIMM:

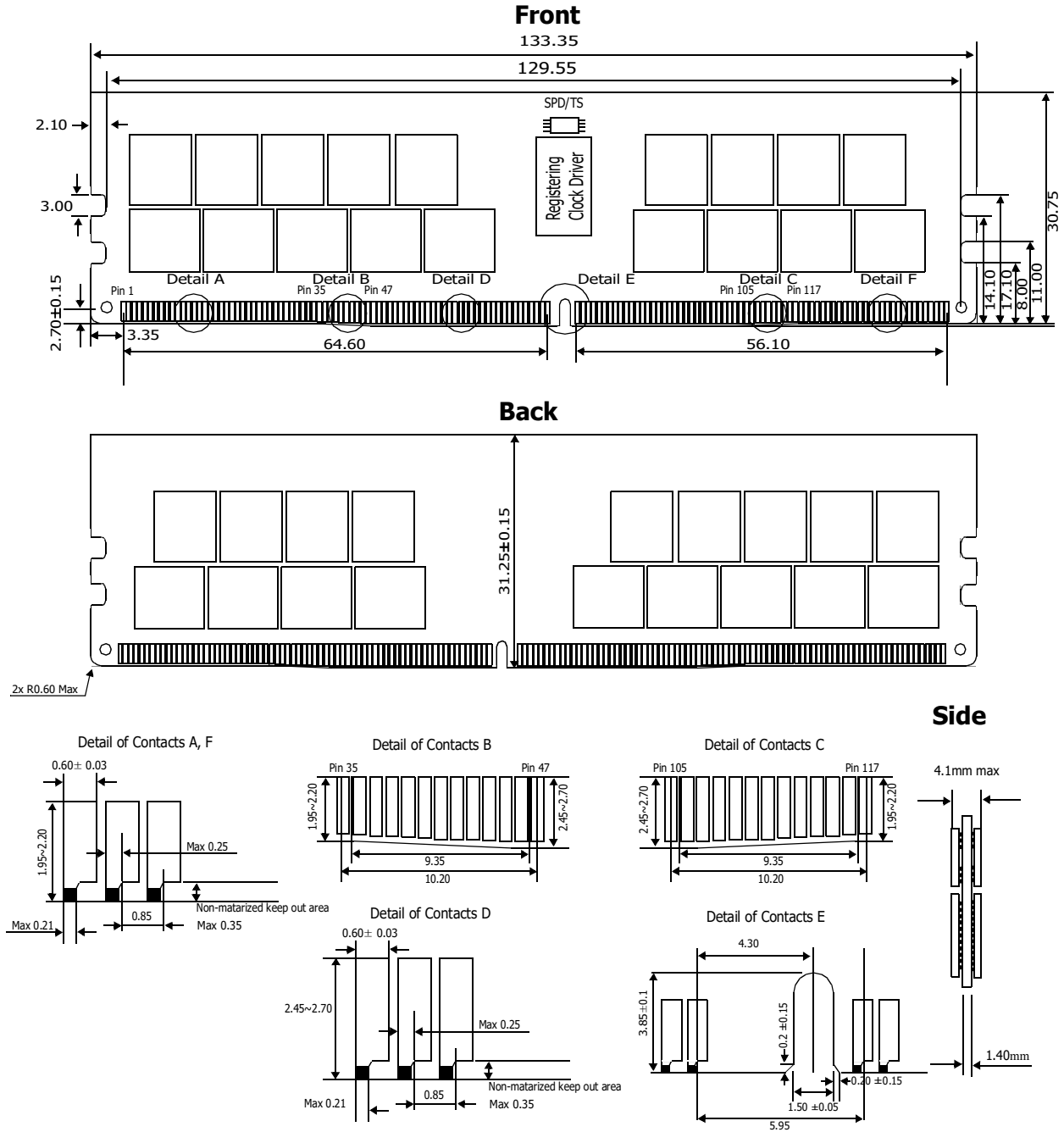
HMAT14JWRRB120N / HMAT14JWRRB122N / HMAT14JXSRB120N / HMAT14JXSRB122N

Symbol	IDD		unit	note
	2933	3200		
IDD0	2220	2270	mA	
IDD0A	2220	2270	mA	
IDD1	2361	2429	mA	
IDD1A	2432	2500	mA	
IDD2N	2105	2154	mA	
IDD2NA	2106	2155	mA	
IDD2NT	2245	2330	mA	
IDD2NL	1708	1757	mA	
IDD2NG	2082	2131	mA	
IDD2ND	1998	2047	mA	
IDD2NP	2022	2107	mA	
IDD2P	1347	1400	mA	
IDD2Q	1936	2021	mA	
IDD3N	2551	2564	mA	
IDD3NA	2523	2572	mA	
IDD3P	1835	1887	mA	
IDD4R	4165	4341	mA	
IDD4RA	4218	4394	mA	
IDD4W	4348	4524	mA	
IDD4WA	4436	4613	mA	
IDD4WC	4231	4389	mA	
IDD4WP	4710	4886	mA	
IDD5B1	15769	15818	mA	
IDD5F2	11245	11294	mA	
IDD5F4	9529	9560	mA	
IDD6N	2810	2810	mA	
IDD6E	4417	4417	mA	
IDD6R	1285	1285	mA	
IDD6A	4427	4427	mA	
IDD7	4893	5177	mA	
IDD8	644	644	mA	

Symbol	IPP		unit	note
	2933	3200		
IPP0	378	378	mA	
IPP1	380	380	mA	
IPP2N	347	347	mA	
IPP2P	283	283	mA	
IPP3N	363	363	mA	
IPP3P	314	314	mA	
IPP4R	419	419	mA	
IPP4W	416	416	mA	
IPP5B1	2832	2832	mA	
IPP5F2	1792	1792	mA	
IPP5F4	1482	1482	mA	
IPP6N	504	504	mA	
IPP6E	788	788	mA	
IPP6R	320	320	mA	
IPP6A	735	735	mA	
IPP7	734	734	mA	
IPP8	284	284	mA	

Module Dimensions

32Gx72 RDIMM : HMAT14JWRRB120N/HMAT14JWRRB122N/HMAT14JXSRB120N/HMAT14JXSRB122N



Note:

1. ±0.13 tolerance on all dimensions unless otherwise stated.
2. The dimensional diagram is for reference only.

Units: millimeters