Commercial Mobile LPDDR3 8Gb / 16Gb(DDP) SDRAM

Features

- **Basis LPDDR3 Compliant**
  - Low Power Consumption
  - 8n Prefetch Architecture and BL8 only
- **Signal Integrity**
  - Configurable DS for system compatibility
  - Configurable On-Die Termination[1]
  - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240Ω± 1%)
- **Training for Signals' Synchronization**
  - DQ Calibration offering specific DQ output patterns
  - CA Training
  - Write Leveling via MR settings [2]
- **Data Integrity**
  - DRAM built-in Temperature Sensor for Temperature Compensated Self Refresh (TCSR)
  - Auto Refresh and Self Refresh Modes
- **Power Saving Modes**
  - Deep Power Down Mode (DPD)
  - Partial Array Self Refresh (PASR)
  - Clock Stop capability during idle period
- **HSUL12 interface and Power Supply**
  - VDD1= 1.70 to 1.95V
  - VDD2/VDDQ/VDDCA = 1.14 to 1.3V

Programmable functions

- **R_{ON} (Typical:34.3/40/48/60/80)**
- **R_{ON} (PD34.3_PU40 / PD40_PU48 / PD34.3_PU48)**
- **R_{TT} (120/240)**
- **RL/WL Select (Set A / Set B)**
- **nWRE (nWR≦9 / nWR>9)**
- **PASR (bank/segment)**

Options

- **Speed Grade (DataRate/Read Latency)**
  - 1866 Mbps / RL=14
- **Temperature Range (*Tc*)**
  - Commercial Grade : - 30℃ to +85℃, extending 105℃[4]

Packages / Density information

Lead-free RoHS compliance and Halogen-free

Items (FBGA Package)	Width x Length x Height (mm)	Ball pitch (mm)
168b PoP	12.00 x 12.00 x 0.83	0.50
178b	10.50 x 11.50 x 0.83	0.65/0.80 Mixed
216b PoP	12.00 x 12.00 x 0.80	0.40
256b PoP	14.00 x 14.00 x 0.80	0.40

Density, Signals and Addressing

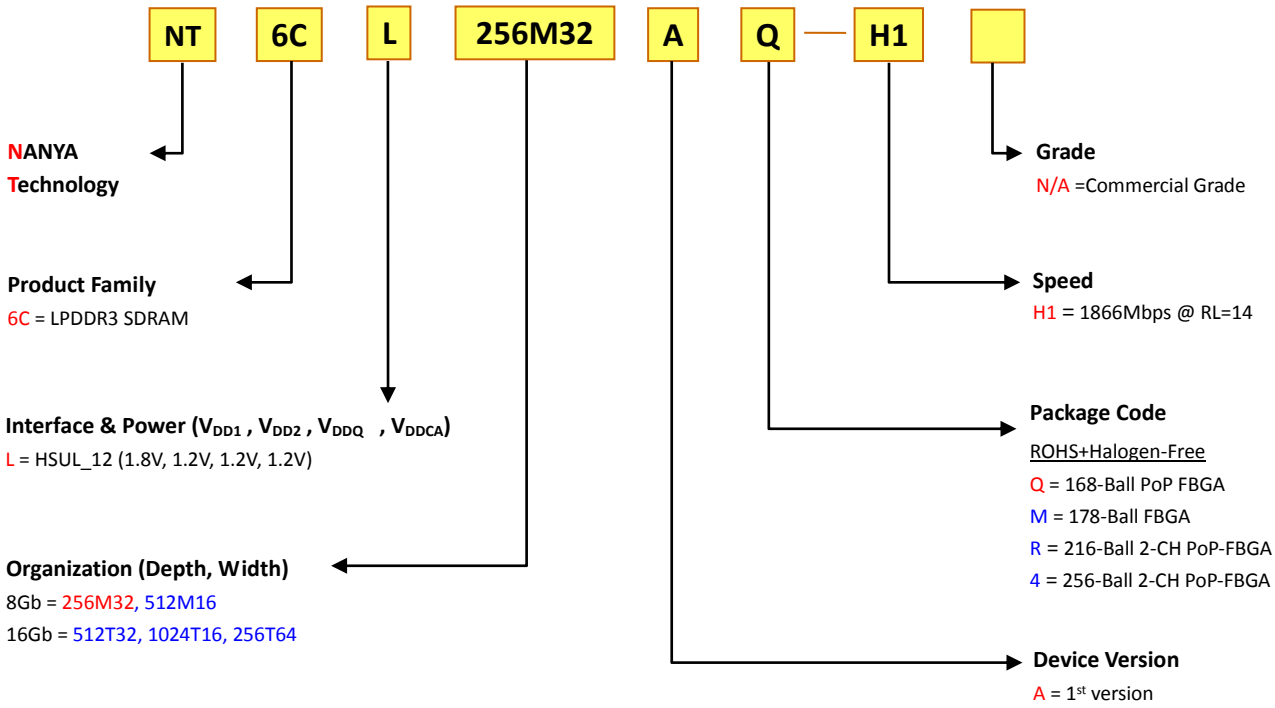
Items	8Gb (SDP)		16Gb (DDP)		
	X16	X32	X16	X32	X64(2ch)
$\overline{CS}$	$\overline{CS}$		$\overline{CS}$[1:0]		$\overline{CS}$_a/b
CK/$\overline{CK}$/CKE	CK / $\overline{CK}$ / CKE		CK / $\overline{CK}$ / CKE[1:0]		CK / $\overline{CK}$ / CKE_a/b
DQ	[15:0]	[31:0]	[15:0]	[31:0]	[31:0] _a/b
DQS/DM	[1:0] / [1:0]	[3:0] / [3:0]	[1:0] / [1:0]	[3:0] / [3:0]	[3:0] _a/b / [3:0] _a/b
CA	CA[9:0]				CA[9:0] _a/b
Bank Addr.	BA[2:0]				
Row Addr.[3]	R[14:0]				
Column Addr.[3]	C[10:0]	C[9:0]	C[10:0]	C[9:0]	C[9:0]
tREFI	3.9μs (Tc≦85℃), 0.975μs (Tc>85℃)				

NOTE 1 Depending on ballout, ODT pin may be NOT supported so ODT die pad is connected to Vss inside the package.
NOTE 2 Write Leveling DQ feedback on all DQs
NOTE 3 Row and Column Addresses values on the CA bus that are not used are "don't care."
NOTE 4 AC/DC will be derated (increased) when above 85℃

Ordering Information

Density	Organization	Part Number	Package	Speed		
				TCK (ns)	Data Rate (Mb/s/pin)	RL
Commercial Grade						
8Gb (SDP)	**256M x 32**	NT6CL256M32AQ-H1	168-Ball PoP	1.07	1866	14
		NT6CL256M32AM-H1	178-Ball	1.07	1866	14
	512M x 16	NT6CL512M16AM-H1		1.07	1866	14
16Gb (DDP)	**512M x 32**	NT6CL512T32AQ-H1	168-Ball PoP	1.07	1866	14
		NT6CL512T32AM-H1	178-Ball	1.07	1866	14
	1024M x 16	NT6CL1024T16AM-H1		1.07	1866	14
	256M x 64 (2-CH)	NT6CL256T64AR-H1	216-Ball PoP	1.07	1866	14
		NT6CL256T64A4-H1	256-Ball PoP	1.07	1866	14

NANYA Mobile LPDDR3 Part Number Naming Guide



NOTE: M=Mono; T=DDP

Operating Frequency

The backward compatibility of each frequency is listed in the following table. If an application operates at specific frequency which is not defined herein but within the highest and the lowest frequencies, then the comparative loose specifications to DRAM must be adopted from the neighboring defined frequency. Please confirm with NTC when the operating frequency is slower than the defined frequency.

Frequency[MHz]	933	800	667	Unit
RL[nCK]	14	12	10	
VDDQ[V]	1.2	1.2	1.2	
NT6CL256M32AQ-H1	1866	1600	1333	Mbps
NT6CL256M32AM-H1				
NT6CL512M16AM-H1				
NT6CL512T32AQ-H1				
NT6CL512T32AM-H1				
NT6CL1024T16AM-H1				
NT6CL256T64AR-H1				
NT6CL256T64A4-H1				

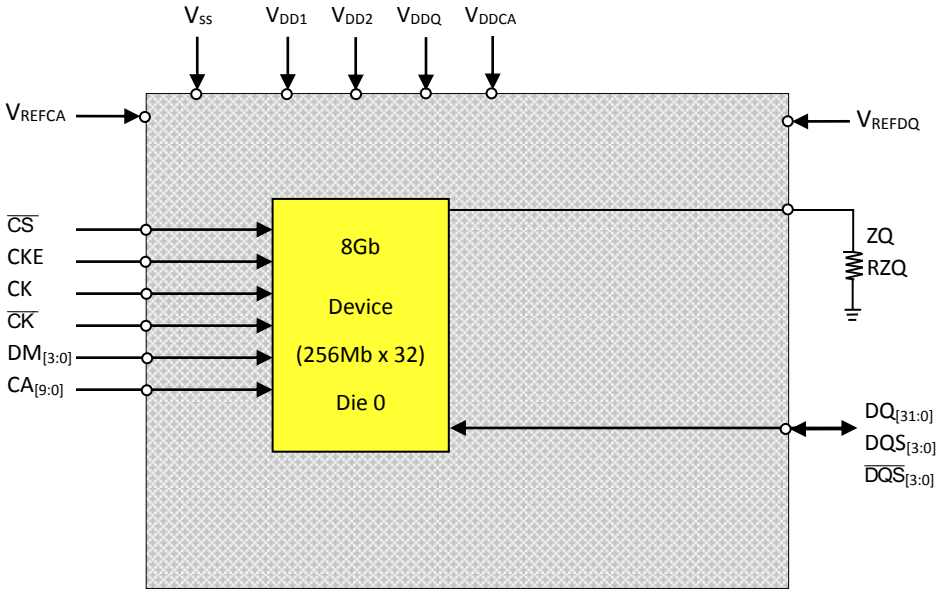
Notes:

These devices also support functional operation at lower frequencies not shown in the table which are not subject to Production Tests but has been verified.

Power, Ground, Signals of Single Die, Single Channel Package

Part Number: NT6CL256M32AQ-XXX

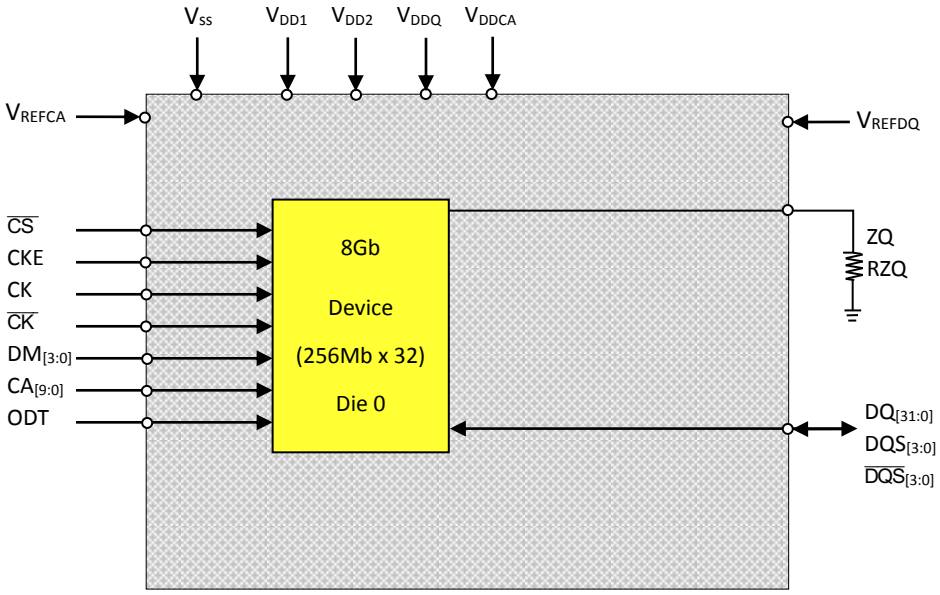
Available: 168b



NOTE 1 ODT pin is NOT supported. ODT die pad is connected to VSS inside the package.

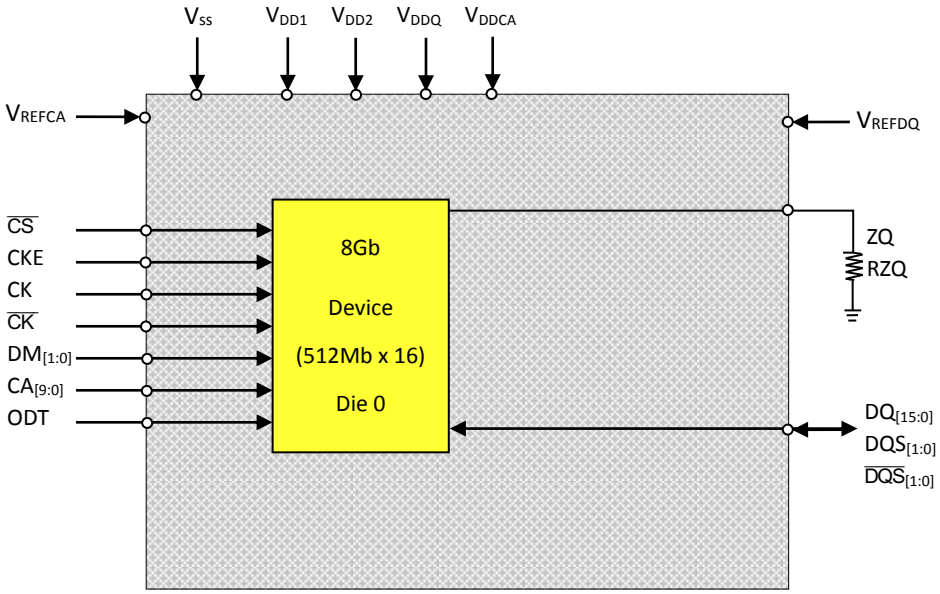
Part Number: NT6CL256M32AM-XXX

Available: 178b



Part Number: NT6CL512M16AM-XXX

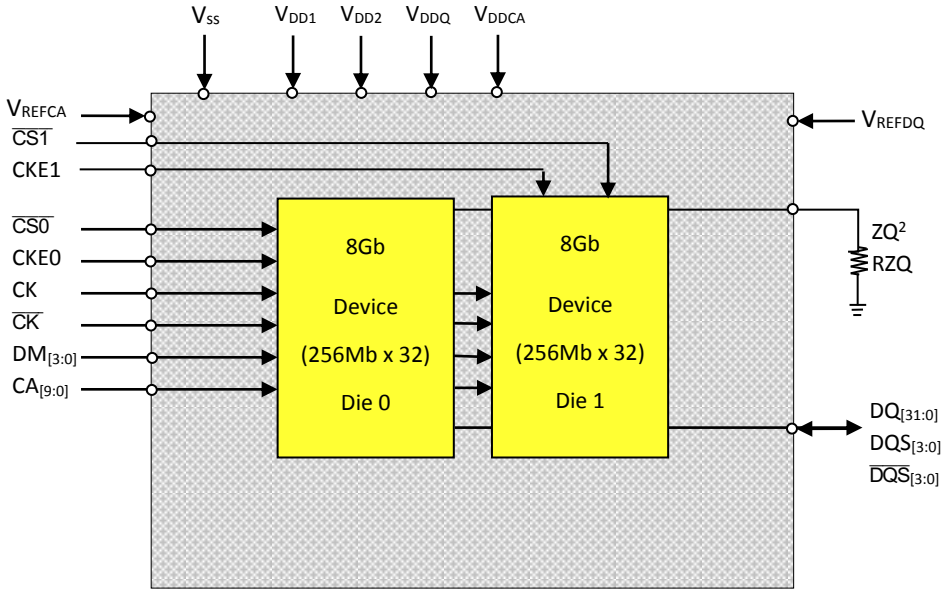
Available: 178b



Power, Ground, Signals of Dual Die, Single Channel Package

Part Number: NT6CL512T32AQ-XXX

Available: 168b

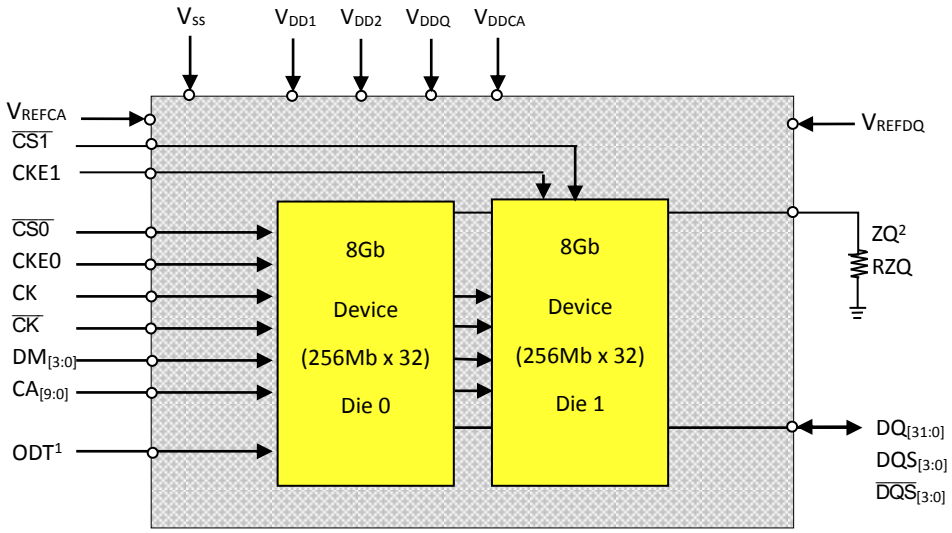


NOTE 1 ODT pins are NOT supported. ODT die pad is connected to VSS inside the package.

NOTE 2 ZQ is connected to both dies.

Part Number: NT6CL512T32AM-XXX

Available: 178b

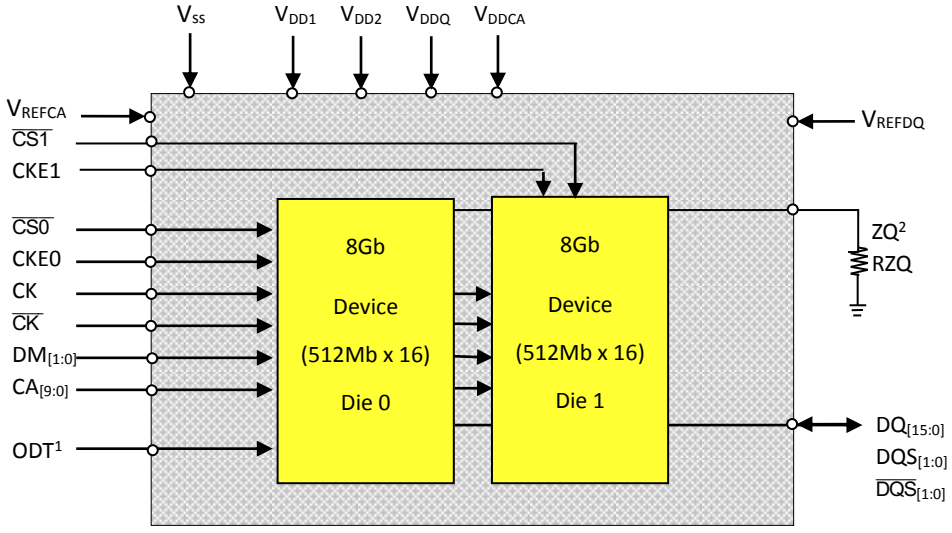


NOTE 1 ODT will be connected to rank0 (die0). The ODT input to rank1 (die1) will be connected to VSS in the package.

NOTE 2 ZQ is connected to both dies.

Part Number: NT6CL1024T16AM-XXX

Available: 178b



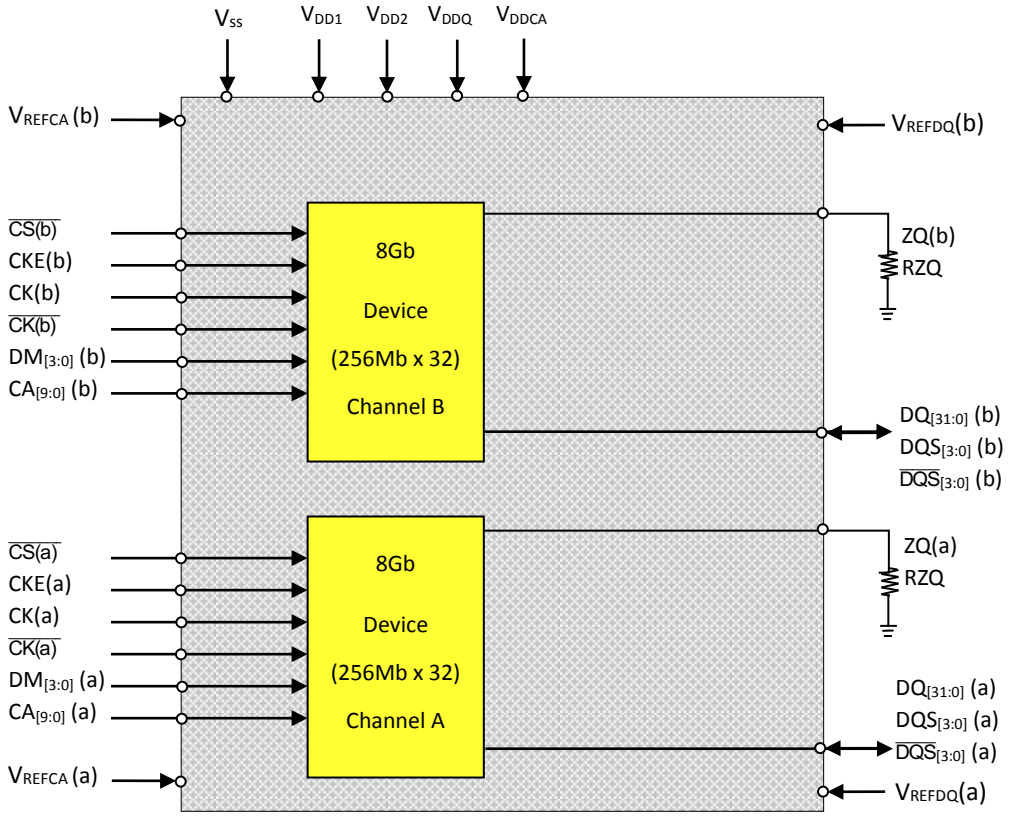
NOTE 1 ODT will be connected to rank0 (die0). The ODT input to rank1 (die1) will be connected to VSS in the package.

NOTE 2 ZQ is connected to both dies.

Power, Ground, Signals of Dual Die, Dual Channel Package

Part Number: NT6CL256T64AR-XXX

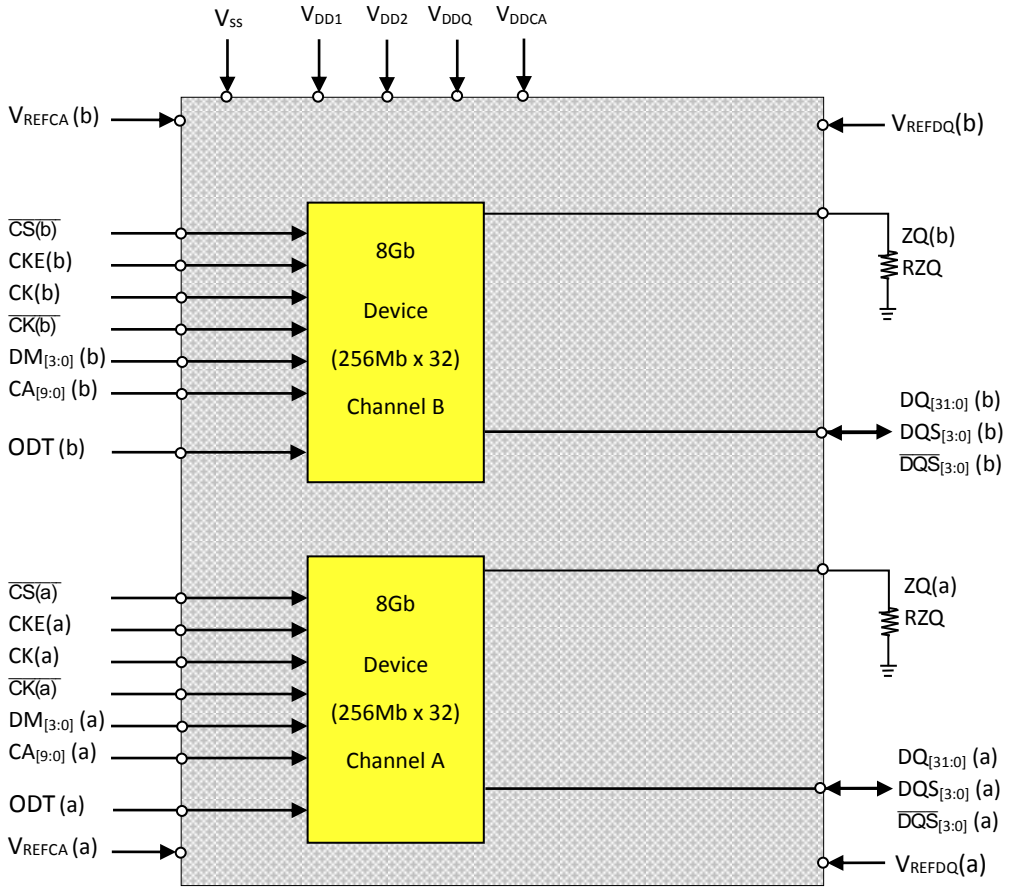
Available: 216b (2-channel)



Power, Ground, Signals of Dual Die, Dual Channel Package

Part Number: NT6CL256T64A4-XXX

Available: 256b (2-channel)



LPDDR3 12x12 PoP-FBGA 1-channel x 32 ballout

(168-ball SDP, 12.00mm x 12.00mm, 0.50mm pitch)

Part Number: NT6CL256M32AQ-XXX

< TOP View>

See the balls through the package

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	VDD1	VSS	DQ30	DQ29	VSS	DQ26	DQ25	VSS	$\overline{DQS3}$	VDD1	VSS	DNU	DNU	A
B	DNU	DNU	VDD1	DNU	DNU	DNU	DNU	DNU	DNU	VSS	VDD2	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3	VDDQ	DM3	VDD2	DNU	DNU	B
C	VSS	VDD2																				DQ15	VSS	C
D	DNU	DNU																				VDDQ	DQ14	D
E	DNU	DNU																				DQ12	DQ13	E
F	DNU	DNU																				DQ11	VSS	F
G	DNU	DNU																				VDDQ	DQ10	G
H	DNU	DNU																				DQ8	DQ9	H
J	DNU	DNU																				DQS1	VSS	J
K	DNU	DNU																				VDDQ	$\overline{DQS1}$	K
L	DNU	DNU																				VDD2	DM1	L
M	DNU	VSS																				VrefDQ	VSS	M
N	DNU	VDD1																				VDD1	DM0	N
P	ZQ	VrefCA																				$\overline{DQS0}$	VSS	P
R	VSS	VDD2																				VDDQ	DQS0	R
T	CA9	CA8																				DQ6	DQ7	T
U	CA7	VDDCA																				DQ5	VSS	U
V	VSS	CA6																				VDDQ	DQ4	V
W	CA5	VDDCA																				DQ2	DQ3	W
Y	$\overline{CK}$	CK																				DQ1	VSS	Y
AA	VSS	VDD2																				VDDQ	DQ0	AA
AB	DNU	DNU	$\overline{CS}$	NC	VDD1	CA1	VSS	CA3	CA4	VDD2	VSS	DQ16	VDDQ	DQ18	DQ20	VDDQ	DQ22	DQS2	VDDQ	DM2	VDD2	DNU	DNU	AB
AC	DNU	DNU	CKE	NC	VSS	CA0	CA2	VDDCA	DNU	DNU	NC	VSS	DQ17	DQ19	VSS	DQ21	DQ23	VSS	$\overline{DQS2}$	VDD1	VSS	DNU	DNU	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

NOTE 1 Do Not Use (DNU)

NOTE 2 Top View, A1 in Top Left Corner

NOTE 3 ODT pin is NOT supported. ODT die pad is connected to VSS inside the package.

LPDDR3 178-ball FBGA SDP X32 ballout

(10.50mm x 11.50mm, 0.65mm/0.80mm mixed pitch)

Part Number: NT6CL256M32AM-XXX

< TOP View>

See the balls through the package

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	A
B	DNU	VSS	ZQ	NC	VSS	VSS		DQ31	DQ30	DQ29	DQ28	VSS	DNU	B
C		CA9	VSS	NC	VSS	VSS		DQ27	DQ26	DQ25	DQ24	VDDQ		C
D		CA8	VSS	VDD2	VDD2	VDD2		DM3	DQ15	DQS3	$\overline{DQS3}$	VSS		D
E		CA7	CA6	VSS	VSS	VSS		VDDQ	DQ14	DQ13	DQ12	VDDQ		E
F		VDDCA	CA5	VSS	VSS	VSS		DQ11	DQ10	DQ9	DQ8	VSS		F
G		VDDCA	VSS	VSS	VDD2	VSS		DM1	VSS	DQS1	$\overline{DQS1}$	VDDQ		G
H		VSS	VDDCA	VREFCA	VDD2	VDD2		VDDQ	VDDQ	VSS	VDDQ	VDD2		H
J		$\overline{CK}$	CK	VSS	VDD2	VDD2		ODT	VDDQ	VDDQ	VREFDQ	VSS		J
K		VSS	CKE	NC	VDD2	VDD2		VDDQ	NC	VSS	VDDQ	VDD2		K
L		VDDCA	$\overline{CS}$	NC	VDD2	VSS		DM0	VSS	DQS0	$\overline{DQS0}$	VDDQ		L
M		VDDCA	CA4	VSS	VSS	VSS		DQ4	DQ5	DQ6	DQ7	VSS		M
N		CA2	CA3	VSS	VSS	VSS		VDDQ	DQ1	DQ2	DQ3	VDDQ		N
P		CA1	VSS	VDD2	VDD2	VDD2		DM2	DQ0	DQS2	$\overline{DQS2}$	VSS		P
R		CA0	NC	VSS	VSS	VSS		DQ20	DQ21	DQ22	DQ23	VDDQ		R
T	DNU	VSS	VSS	VSS	VSS	VSS		DQ16	DQ17	DQ18	DQ19	VSS	DNU	T
U	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	

NOTE 1 Do Not Use (DNU)

NOTE 2 Top View, A1 in Top Left Corner

LPDDR3 178-ball FBGA SDP X16 ballout

(10.50mm x 11.50mm, 0.65mm/0.80mm mixed pitch)

Part Number: NT6CL512M16AM-XXX

< TOP View>

See the balls through the package

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	A
B	DNU	VSS	ZQ	NC	VSS	VSS		NC	NC	NC	NC	VSS	DNU	B
C		CA9	VSS	NC	VSS	VSS		NC	NC	NC	NC	VDDQ		C
D		CA8	VSS	VDD2	VDD2	VDD2		NC	DQ15	NC	NC	VSS		D
E		CA7	CA6	VSS	VSS	VSS		VDDQ	DQ14	DQ13	DQ12	VDDQ		E
F		VDDCA	CA5	VSS	VSS	VSS		DQ11	DQ10	DQ9	DQ8	VSS		F
G		VDDCA	VSS	VSS	VDD2	VSS		DM1	VSS	DQS1	$\overline{DQS1}$	VDDQ		G
H		VSS	VDDCA	VREFCA	VDD2	VDD2		VDDQ	VDDQ	VSS	VDDQ	VDD2		H
J		$\overline{CK}$	CK	VSS	VDD2	VDD2		ODT	VDDQ	VDDQ	VREFDQ	VSS		J
K		VSS	CKE	NC	VDD2	VDD2		VDDQ	NC	VSS	VDDQ	VDD2		K
L		VDDCA	$\overline{CS}$	NC	VDD2	VSS		DM0	VSS	DQS0	$\overline{DQS0}$	VDDQ		L
M		VDDCA	CA4	VSS	VSS	VSS		DQ4	DQ5	DQ6	DQ7	VSS		M
N		CA2	CA3	VSS	VSS	VSS		VDDQ	DQ1	DQ2	DQ3	VDDQ		N
P		CA1	VSS	VDD2	VDD2	VDD2		NC	DQ0	NC	NC	VSS		P
R		CA0	NC	VSS	VSS	VSS		NC	NC	NC	NC	VDDQ		R
T	DNU	VSS	VSS	VSS	VSS	VSS		NC	NC	NC	NC	VSS	DNU	T
U	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	

NOTE 1 Do Not Use (DNU)

NOTE 2 Top View, A1 in Top Left Corner

LPDDR3 12x12 PoP-FBGA 1-channel x 32 ballout

(168-ball DDP, 12.00mm x 12.00mm, 0.50mm pitch)

Part Number: NT6CL512T32AQ-XXX

< TOP View>

See the balls through the package

A1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	VDD1	VSS	DQ30	DQ29	VSS	DQ26	DQ25	VSS	$\overline{DQS3}$	VDD1	VSS	DNU	DNU	A
B	DNU	DNU	VDD1	DNU	DNU	DNU	DNU	DNU	DNU	VSS	VDD2	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3	VDDQ	DM3	VDD2	DNU	DNU	B
C	VSS	VDD2																				DQ15	VSS	C
D	DNU	DNU																				VDDQ	DQ14	D
E	DNU	DNU																				DQ12	DQ13	E
F	DNU	DNU																				DQ11	VSS	F
G	DNU	DNU																				VDDQ	DQ10	G
H	DNU	DNU																				DQ8	DQ9	H
J	DNU	DNU																				DQS1	VSS	J
K	DNU	DNU																				VDDQ	$\overline{DQS1}$	K
L	DNU	DNU																				VDD2	DM1	L
M	DNU	VSS																				VrefDQ	VSS	M
N	DNU	VDD1																				VDD1	DM0	N
P	ZQ	VrefCA																				$\overline{DQS0}$	VSS	P
R	VSS	VDD2																				VDDQ	DQS0	R
T	CA9	CA8																				DQ6	DQ7	T
U	CA7	VDDCA																				DQ5	VSS	U
V	VSS	CA6																				VDDQ	DQ4	V
W	CA5	VDDCA																				DQ2	DQ3	W
Y	$\overline{CK}$	CK																				DQ1	VSS	Y
AA	VSS	VDD2																				VDDQ	DQ0	AA
AB	DNU	DNU	$\overline{CS0}$	$\overline{CST}$	VDD1	CA1	VSS	CA3	CA4	VDD2	VSS	DQ16	VDDQ	DQ18	DQ20	VDDQ	DQ22	DQS2	VDDQ	DM2	VDD2	DNU	DNU	AB
AC	DNU	DNU	CKE0	CKE1	VSS	CA0	CA2	VDDCA	DNU	DNU	NC	VSS	DQ17	DQ19	VSS	DQ21	DQ23	VSS	$\overline{DQS2}$	VDD1	VSS	DNU	DNU	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

NOTE 1 Do Not Use (DNU)

NOTE 2 Top View, A1 in Top Left Corner

NOTE 3 ODT pins are NOT supported. ODT die pad is connected to VSS inside the package.

NOTE 4 ZQ is connected to both dies.

LPDDR3 178-ball FBGA DDP X32 ballout

(10.50mm x 11.50mm, 0.65mm/0.80mm mixed pitch)

Part Number: NT6CL512T32AM-XXX

< TOP View>

See the balls through the package

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	A
B	DNU	VSS	ZQ	NC	VSS	VSS		DQ31	DQ30	DQ29	DQ28	VSS	DNU	B
C		CA9	VSS	NC	VSS	VSS		DQ27	DQ26	DQ25	DQ24	VDDQ		C
D		CA8	VSS	VDD2	VDD2	VDD2		DM3	DQ15	DQS3	$\overline{DQS3}$	VSS		D
E		CA7	CA6	VSS	VSS	VSS		VDDQ	DQ14	DQ13	DQ12	VDDQ		E
F		VDDCA	CA5	VSS	VSS	VSS		DQ11	DQ10	DQ9	DQ8	VSS		F
G		VDDCA	VSS	VSS	VDD2	VSS		DM1	VSS	DQS1	$\overline{DQS1}$	VDDQ		G
H		VSS	VDDCA	VREFCA	VDD2	VDD2		VDDQ	VDDQ	VSS	VDDQ	VDD2		H
J		$\overline{CK}$	CK	VSS	VDD2	VDD2		ODT	VDDQ	VDDQ	VREFDQ	VSS		J
K		VSS	CKE0	CKE1	VDD2	VDD2		VDDQ	NC	VSS	VDDQ	VDD2		K
L		VDDCA	$\overline{CS0}$	$\overline{CS1}$	VDD2	VSS		DM0	VSS	DQS0	$\overline{DQS0}$	VDDQ		L
M		VDDCA	CA4	VSS	VSS	VSS		DQ4	DQ5	DQ6	DQ7	VSS		M
N		CA2	CA3	VSS	VSS	VSS		VDDQ	DQ1	DQ2	DQ3	VDDQ		N
P		CA1	VSS	VDD2	VDD2	VDD2		DM2	DQ0	DQS2	$\overline{DQS2}$	VSS		P
R		CA0	NC	VSS	VSS	VSS		DQ20	DQ21	DQ22	DQ23	VDDQ		R
T	DNU	VSS	VSS	VSS	VSS	VSS		DQ16	DQ17	DQ18	DQ19	VSS	DNU	T
U	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	

NOTE 1 Do Not Use (DNU)

NOTE 2 Top View, A1 in Top Left Corner

LPDDR3 178-ball FBGA DDP X16 ballout

(10.50mm x 11.50mm, 0.65mm/0.80mm mixed pitch)

Part Number: NT6CL1024T16AM-XXX

< TOP View>

See the balls through the package

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	A
B	DNU	VSS	ZQ	NC	VSS	VSS		NC	NC	NC	NC	VSS	DNU	B
C		CA9	VSS	NC	VSS	VSS		NC	NC	NC	NC	VDDQ		C
D		CA8	VSS	VDD2	VDD2	VDD2		NC	DQ15	NC	NC	VSS		D
E		CA7	CA6	VSS	VSS	VSS		VDDQ	DQ14	DQ13	DQ12	VDDQ		E
F		VDDCA	CA5	VSS	VSS	VSS		DQ11	DQ10	DQ9	DQ8	VSS		F
G		VDDCA	VSS	VSS	VDD2	VSS		DM1	VSS	DQS1	$\overline{\text{DQS1}}$	VDDQ		G
H		VSS	VDDCA	VREFCA	VDD2	VDD2		VDDQ	VDDQ	VSS	VDDQ	VDD2		H
J		$\overline{\text{CK}}$	CK	VSS	VDD2	VDD2		ODT	VDDQ	VDDQ	VREFDQ	VSS		J
K		VSS	CKE0	CKE1	VDD2	VDD2		VDDQ	NC	VSS	VDDQ	VDD2		K
L		VDDCA	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	VDD2	VSS		DM0	VSS	DQS0	$\overline{\text{DQS0}}$	VDDQ		L
M		VDDCA	CA4	VSS	VSS	VSS		DQ4	DQ5	DQ6	DQ7	VSS		M
N		CA2	CA3	VSS	VSS	VSS		VDDQ	DQ1	DQ2	DQ3	VDDQ		N
P		CA1	VSS	VDD2	VDD2	VDD2		NC	DQ0	NC	NC	VSS		P
R		CA0	NC	VSS	VSS	VSS		NC	NC	NC	NC	VDDQ		R
T	DNU	VSS	VSS	VSS	VSS	VSS		NC	NC	NC	NC	VSS	DNU	T
U	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	U

NOTE 1 Do Not Use (DNU)

NOTE 2 Top View, A1 in Top Left Corner

LPDDR3 12x12 PoP-FBGA 2-channel 2x32 ballout

(216-ball DDP, 12.00mm x 12.00mm, 0.40mm pitch)

Part Number: NT6CL256T64AR-XXX

< TOP View>

See the balls through the package

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	NC	VSS	VDD2	DQ30_a	DQ29_a	VSS	DQ26_a	DQ25_a	VSS	DQS3_a	VSS	DQ14_a	DQ13_a	VSS	VDD1	VDD2	DQ11_a	DQ10_a	DQ9_a	DQS1_a	DM1_a	VDDQ	DQS0_a	DQ7_a	DQ6_a	DQ4_a	DQ3_a	VSS	NC	A
B	VSS	NC	DQ31_a	VDDQ	DQ28_a	DQ27_a	VDDQ	DQ24_a	VDDQ	DQS3_a	DM3_a	DQ15_a	VDDQ	VSS	VREF DQ_a	VDD2	DQ12_a	VDDQ	DQ8_a	/DQS1_a	VSS	DM0_a	/DQS0_a	VSS	VDDQ	DQ5_a	DQ2_a	NC	VSS	B
C	VDD1	DQ16_b																										VDD1	VDD2	C
D	DQ17_b	VDDQ																										DQ1_a	VDDQ	D
E	DQ18_b	DQ19_b																										VSS	DQ0_a	E
F	VSS	DQ20_b																										DM2_a	VDDQ	F
G	DQ21_b	VDDQ																										DQS2_a	DQS2_a	G
H	DQ22_b	DQ23_b																										VSS	DQ23_a	H
J	VSS	VDDQ																										VDDQ	DQ22_a	J
K	DQS2_b	DQS2_b																										DQ20_a	DQ21_a	K
L	DM2_b	DQ0_b																										DQ19_a	VSS	L
M	DQ1_b	VSS																										VDDQ	DQ18_a	M
N	DQ2_b	VDD1																										DQ16_a	DQ17_a	N
P	VSS	VSS																										VDD2	VDD1	P
R	VDD1	VREF DQ_b																										VSS	CA0_b	R
T	VDD2	VDD2																										VDD CA	CA1_b	T
U	VDDQ	DQ3_b																										VREF CA_b	CA2_b	U
V	DQ4_b	VSS																										VSS	CA3_b	V
W	DQ6_b	DQ5_b																										CA4_b	NC	W
Y	VDDQ	DQ7_b																										CS_b	NC	Y
AA	DQS0_b	DQS0_b																										VSS	CKE_b	AA
AB	DM0_b	VSS																										CK_b	CK_b	AB
AC	VDDQ	DM1_b																										VDD CA	CA5_b	AC
AD	DQS1_b	DQS1_b																										CA7_b	CA6_b	AD
AE	DQ8_b	VSS																										CA8_b	VDD CA	AE
AF	DQ9_b	VDDQ																										VSS	CA9_b	AF
AG	DQ10_b	DQ11_b																										VDD2	ZQ_b	AG
AH	VSS	VDD1	VDD2	DQ13_b	VSS	DQ15_b	DM3_b	DQS3_b	VDDQ	DQ26_b	DQ27_b	VDDQ	DQ30_b	VSS	VDD2	VREF CA_a	CA9_a	VSS	CA7_a	CA6_a	CK_a	VDD CA	CKE_a	CS_a	CA3_a	CA2_a	CA1_a	VDD1	VSS	AH
AJ	NC	VSS	DQ12_b	VDDQ	DQ14_b	VDDQ	VSS	DQS3_b	DQ24_b	DQ25_b	VSS	DQ28_b	DQ29_b	DQ31_b	VDD1	VSS	ZQ_a	CA8_a	VDD CA	CA5_a	CK_a	VSS	NC	NC	CA4_a	VDD CA	CA0_a	VSS	NC	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

NOTE 1 Top View, A1 in Top Left Corner

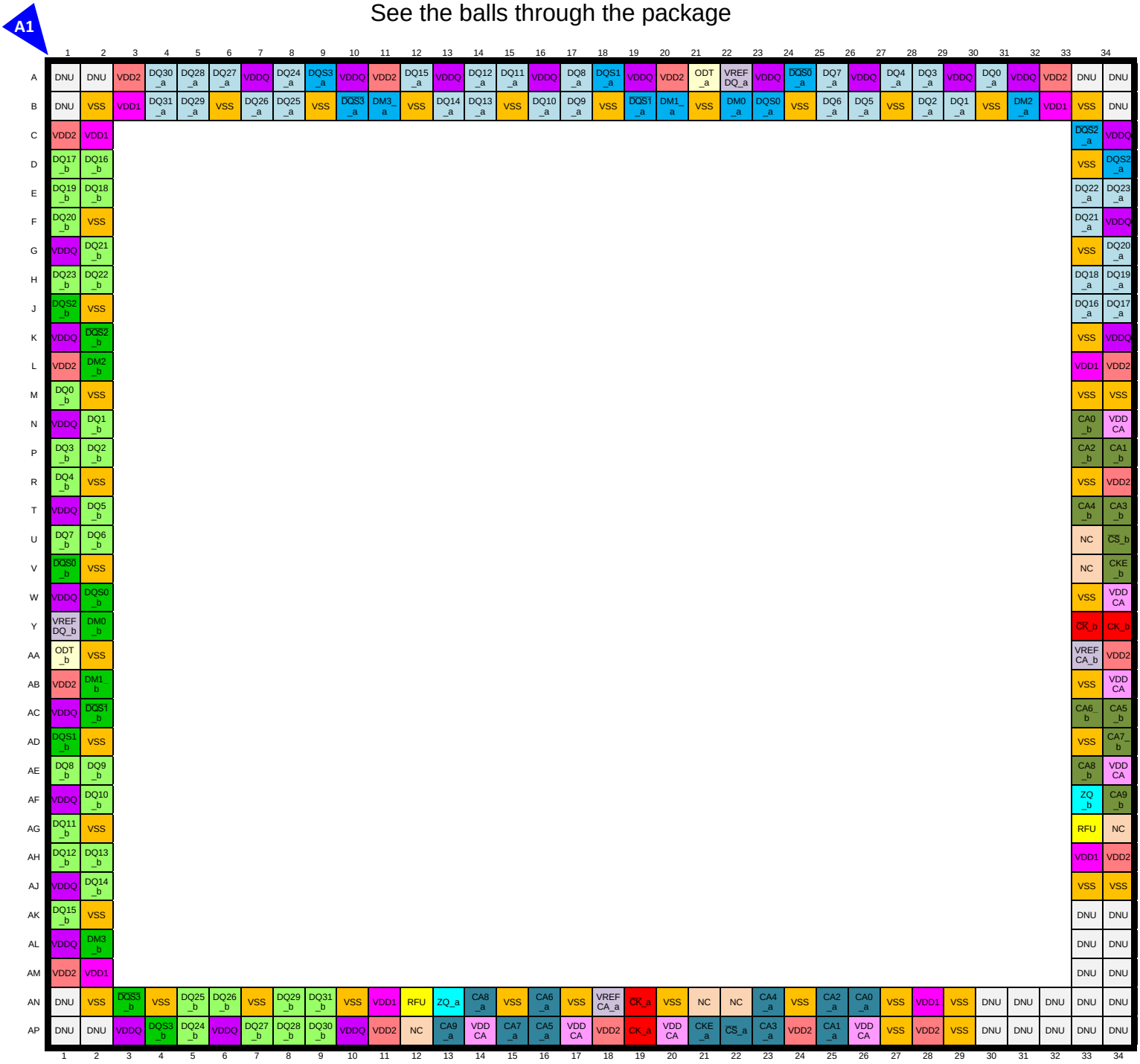
LPDDR3 14x14 PoP-FBGA 2-channel 2x32 ballout

(256-ball DDP, 14.00mm x 14.00mm, 0.40mm pitch)

Part Number: NT6CL256T64A4-XXX

< TOP View>

See the balls through the package



NOTE 1 Do Not Use (DNU)

NOTE 2 Top View, A1 in Top Left Corner

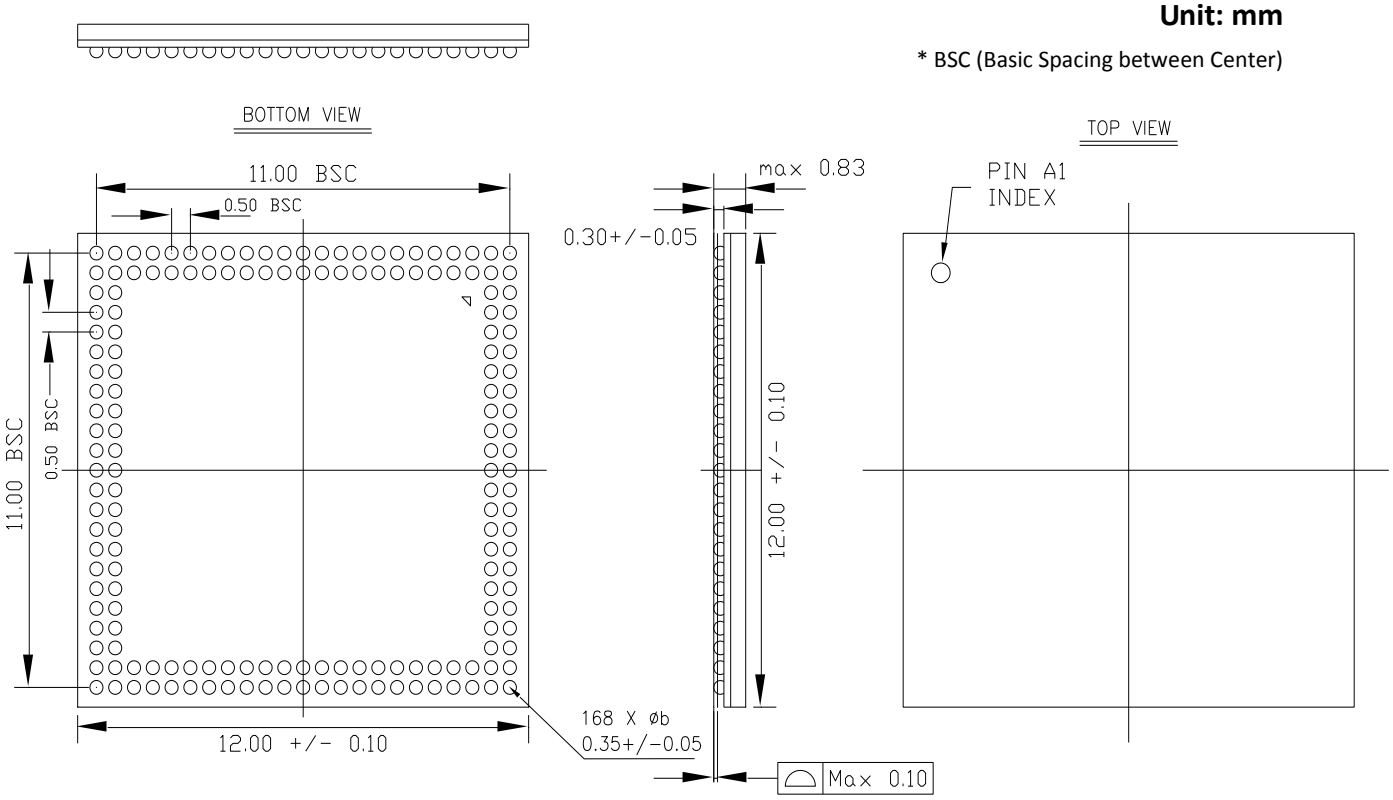
NOTE 3 In case ODT function is not used, ODT pin should be considerd as NC.

168-ball Package Outline Drawing

Part Number: NT6CL256M32AQ-XXX, NT6CL512T32AQ-XXX

Unit: mm

* BSC (Basic Spacing between Center)



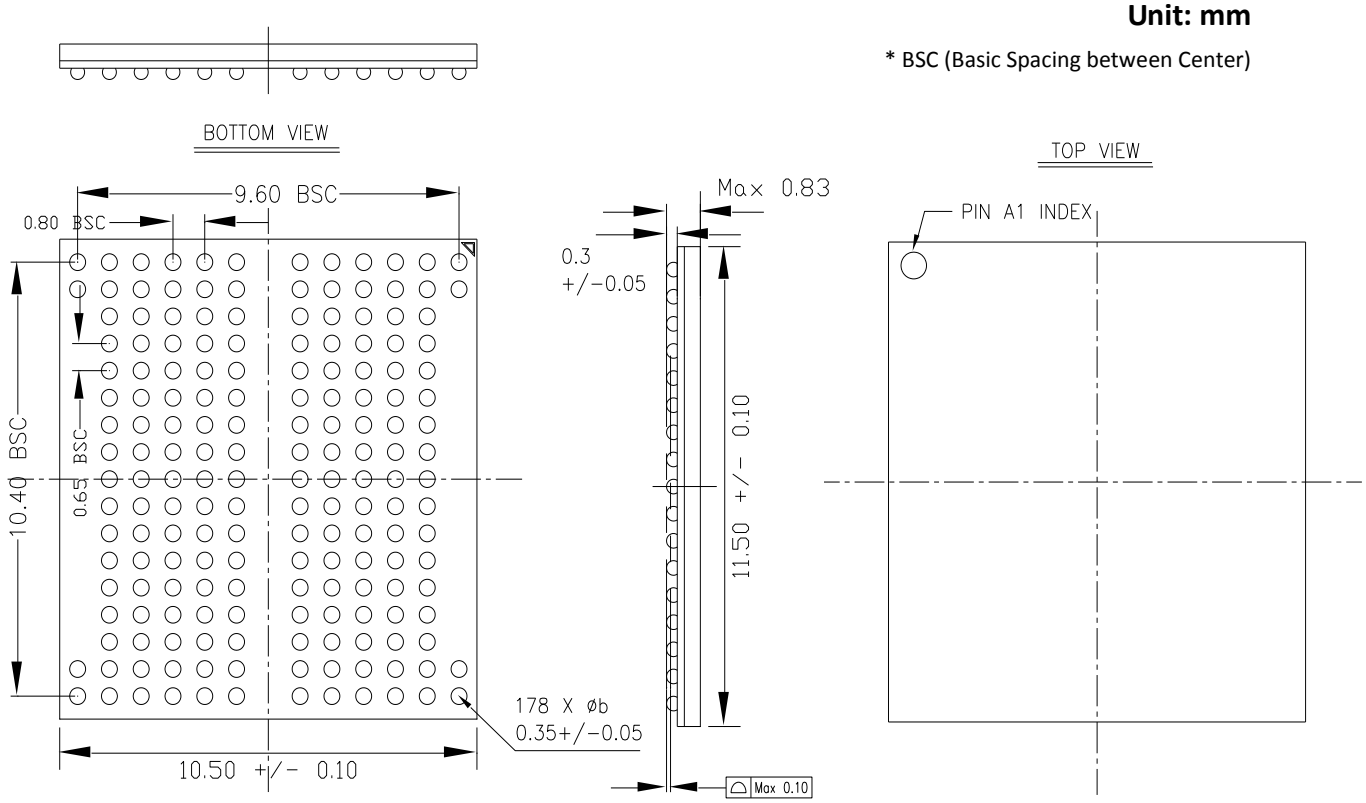
178-ball Package Outline Drawing

Part Number: NT6CL256M32AM-XXX, NT6CL512T32AM-XXX

NT6CL512M16AM-XXX, NT6CL1024T16AM-XXX

Unit: mm

* BSC (Basic Spacing between Center)

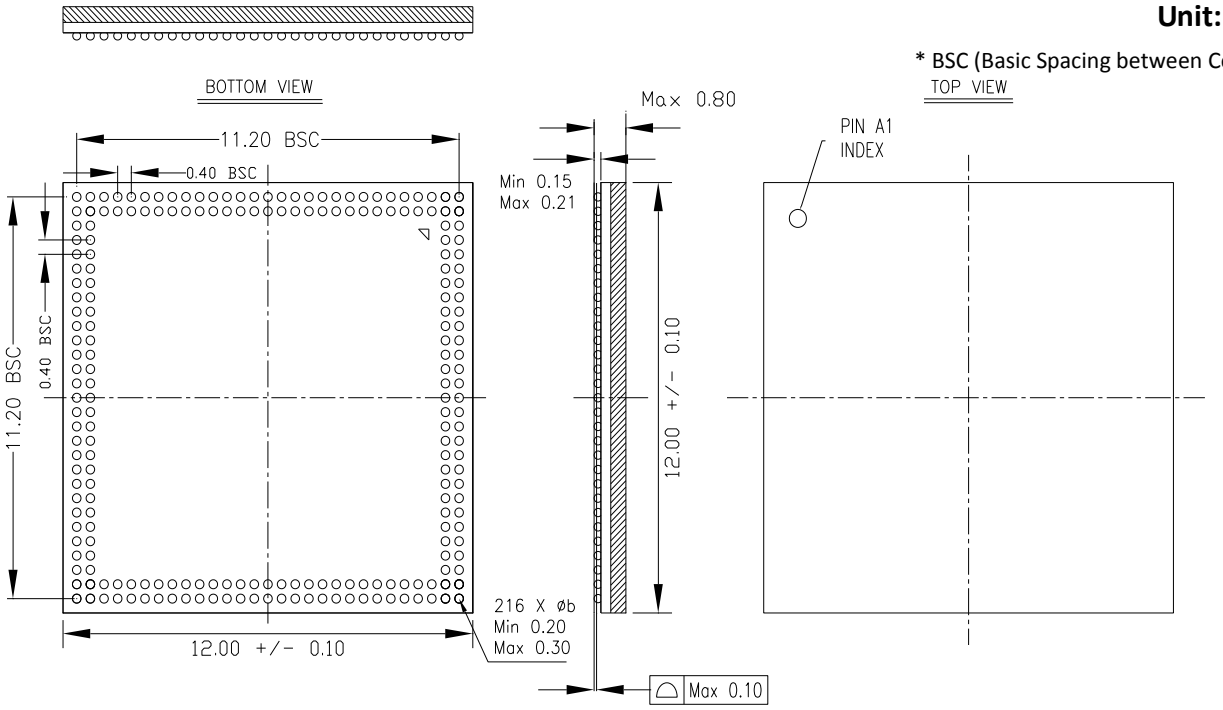


216-ball Package Outline Drawing

Part Number: NT6TL256T64AR-XXX

Unit: mm

* BSC (Basic Spacing between Center)

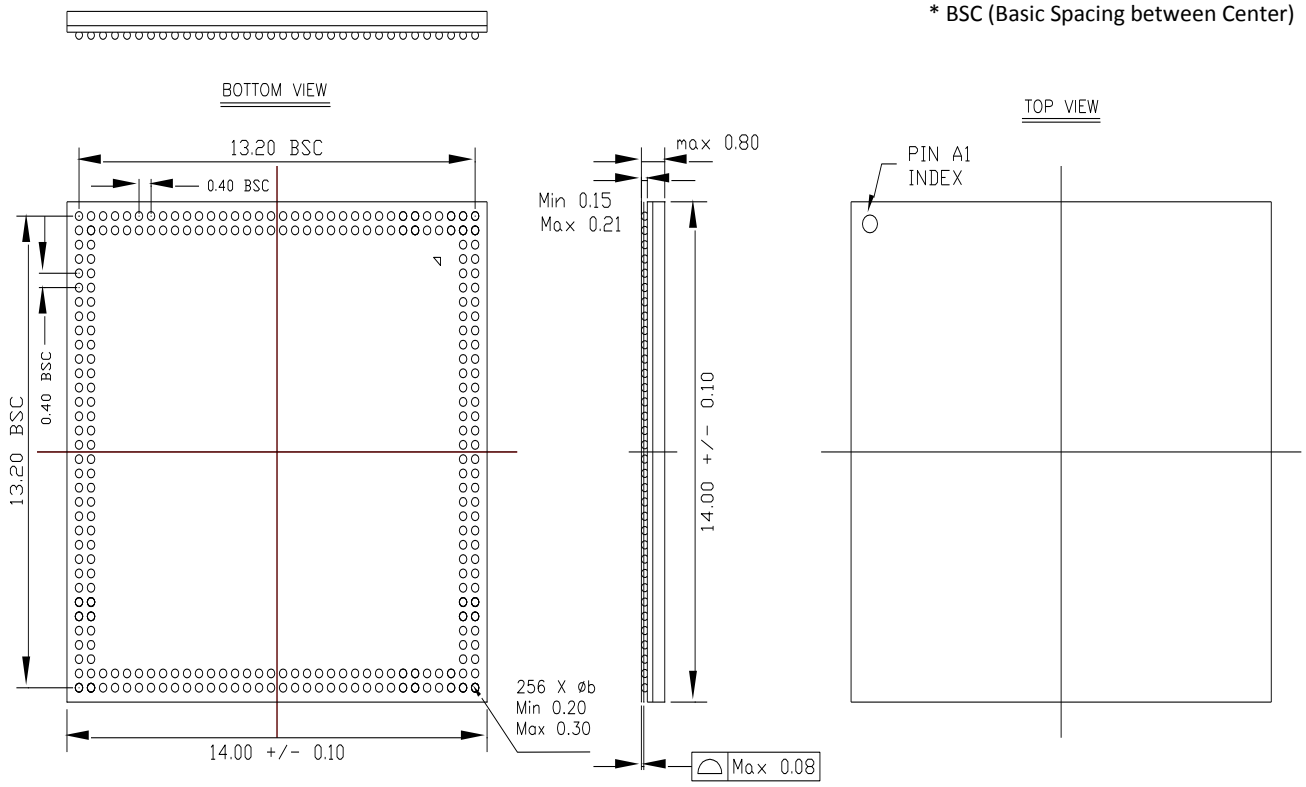


256-ball Package Outline Drawing (14.00mm x 14.00mm)

Part Number: NT6CL256T64A4-XXX

Unit: mm

* BSC (Basic Spacing between Center)



Ball Definition and Descriptions

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK. Single Data Rate (SDR) inputs, $\overline{CS}$ and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK and $\overline{CK}$. The positive Clock edge is defined by the crosspoint of a rising CK and a falling $\overline{CK}$. The negative Clock edge is defined by the crosspoint of a falling CK and a rising $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. CKE is sampled at the positive Clock edge.
$\overline{CS}$	Input	**Chip Select:** $\overline{CS}$ is considered part of the command code. See Command Truth Table for command code descriptions. $\overline{CS}$ is sampled at the positive Clock edge.
CA0 – CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table for command code descriptions.
For x16 DM0 – DM1 For x32 DM0 - DM3	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is for input only, the DM loading shall match the DQ and DQS (or $\overline{DQS}$). For x16 and x32 devices, DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
For x16 DQ0 - DQ15 For x32 DQ0 - DQ31	Input/output	**Data Inputs/Output:** Bi-directional data bus
For x16 DQS0-1, $\overline{DQS0\text{-}1}$ For x32 DQS0-3, $\overline{DQS0\text{-}3}$	Input/output	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS and $\overline{DQS}$). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. For x16 DQS0 and $\overline{DQS0}$ correspond to the data on DQ0 - DQ7, DQS1 and $\overline{DQS1}$ to the data on DQ8 - DQ15, For x32 DQS0 and $\overline{DQS0}$ correspond to the data on DQ0 - DQ7, DQS1 and $\overline{DQS1}$ to the data on DQ8 - DQ15, DQS2 and $\overline{DQS2}$ to the data on DQ16 - DQ23, DQS3 and $\overline{DQS3}$ to the data on DQ24 - DQ31.
ODT	Input	On-Die Termination**:** This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings.

Symbol	Type	Function
ZQ	Reference	**External Reference ball for ZQ Calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SS}.
V_{DD1}	Supply	**Core Power Supply 1:** Core power supply
V_{DD2}	Supply	**Core Power Supply 2:** Core power supply
V_{DDQ}	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
V_{DDCA}	Supply	**Input Receiver Power Supply:** Power supply for CA0-9, CKE, $\overline{CS}$, CK, and $\overline{CK}$ input buffers.
V_{REFCA}	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA0-9, CKE, $\overline{CS}$, CK, and $\overline{CK}$ input buffers.
V_{REFDQ}	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all data input buffers.
V_{SS}	Supply	**Ground**
NC	-	**No Connect: No internal electrical connection is present.**

NOTE 1: The signal may show up in a different symbol but it indicates to the same thing. e.g., /CK = CK# = $\overline{CK}$ = CKb = CK_n = CK_c, /DQS = DQS# = $\overline{DQS}$ = DQSb = DQS_n = DQS_c, /CS = CS# = $\overline{CS}$ = CSb = CS_n.

NOTE 2: Data includes DQ and DM.

Functional Descriptions

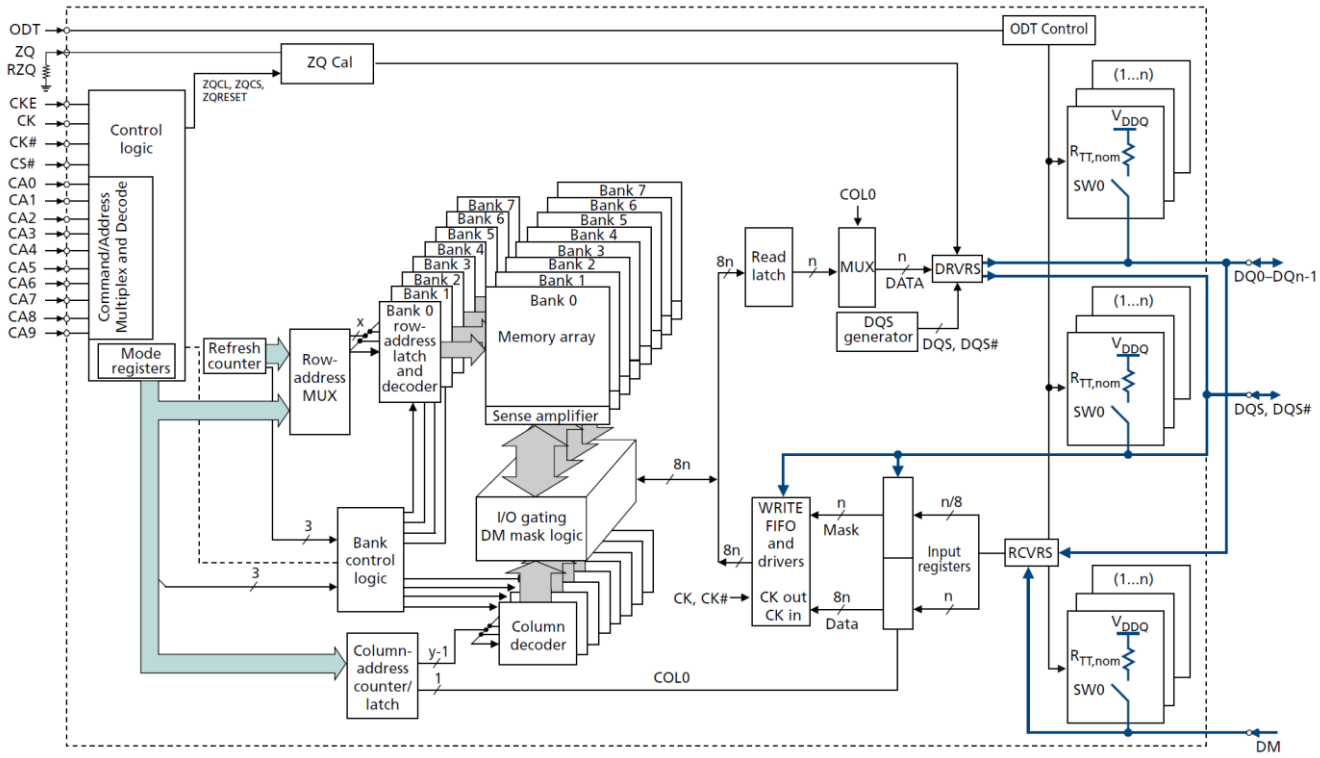
8Gb LPDDR3-SDRAM has 8,589,934,592 bits and 16Gb LPDDR3-SDRAM has 17,179,869,184 bits. These devices are high-speed synchronous DRAM devices internally configured as an 8-bank memory and use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 8n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the device effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the device must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

Functional Block Diagram

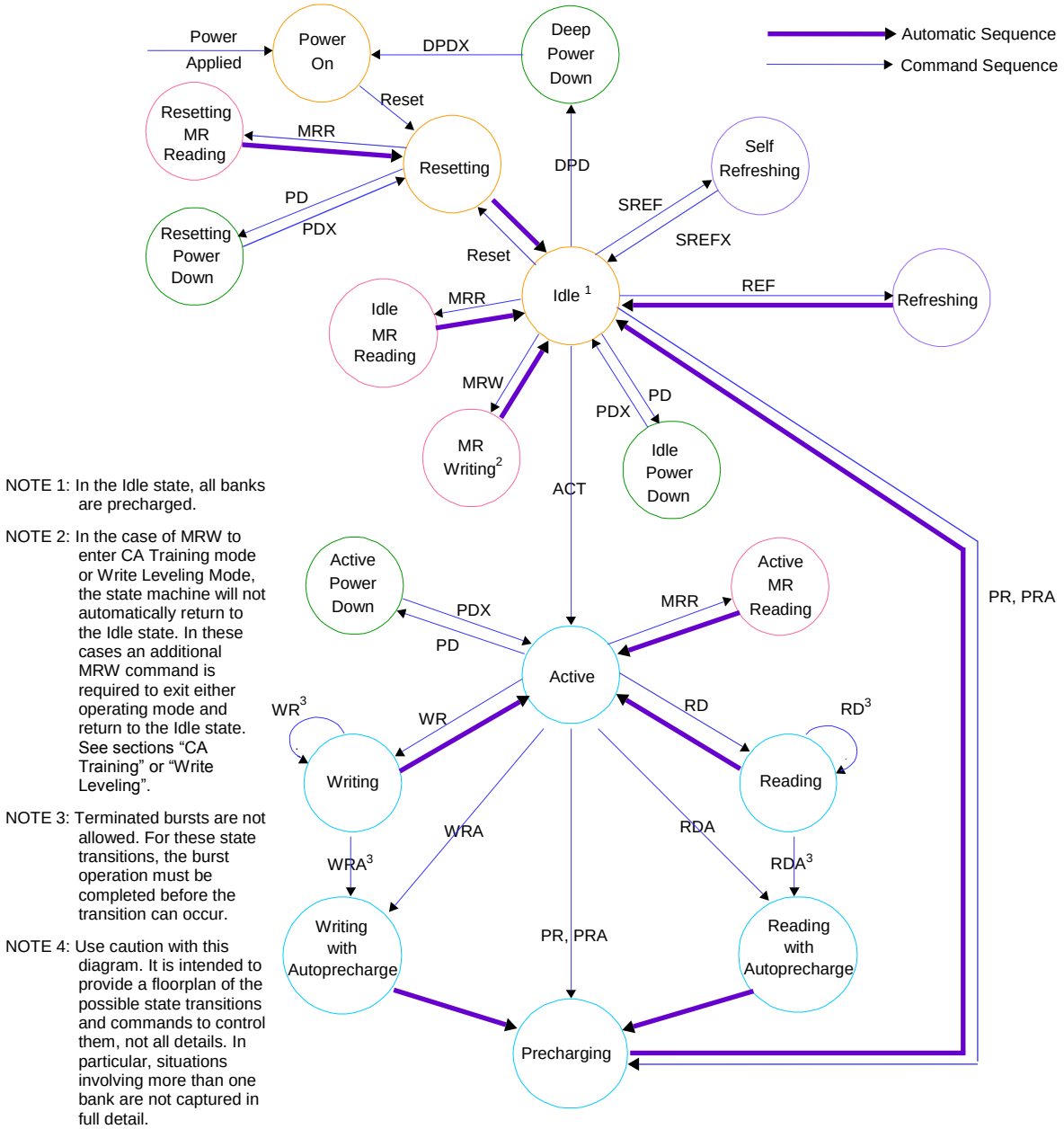


Simplified Bus Interface State Diagram

LPDDR3-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

Simplified State Diagram



NOTE 1: In the Idle state, all banks are precharged.

NOTE 2: In the case of MRW to enter CA Training mode or Write Leveling Mode, the state machine will not automatically return to the Idle state. In these cases an additional MRW command is required to exit either operating mode and return to the Idle state. See sections “CA Training” or “Write Leveling”.

NOTE 3: Terminated bursts are not allowed. For these state transitions, the burst operation must be completed before the transition can occur.

NOTE 4: Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one bank are not captured in full detail.

Abbr.	Function	Abbr.	Function	Abbr.	Function
ACT	Active	**PD**	Enter Power Down	**SREF**	Enter self refresh
RD(A)	Read (w/ Autoprecharge)	**PDX**	Exit Power Down	**SREFX**	Exit self refresh
WR(A)	Write (w/ Autoprecharge)	**DPD**	Enter Deep Power Down		
PR(A)	Precharge (All)	**DPDX**	Exit Deep Power Down		
MRW	Mode Register Write	**REF**	Refresh		
MRR	Mode Register Read	**RESET**	Reset is achieved through MRW command		

Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	-0.4	2.3	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	-0.4	1.6	V	1
V_{DDCA} supply voltage relative to V_{SS}	V_{DDCA}	-0.4	1.6	V	1,2
V_{DDQ} supply voltage relative to V_{SS}	V_{DDQ}	-0.4	1.6	V	1,3
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.6	V	
Storage Temperature	T_{STG}	-55	125	°C	4

NOTE 1 See “Power-Ramp” section for relationships between power supplies.

NOTE 2 $V_{REFCA} \leq 0.6 \times V_{DDCA}$; however, V_{REFCA} may be $\geq V_{DDCA}$ provided that $V_{REFCA} \leq 300mV$.

NOTE 3 $V_{REFDQ} \leq 0.7 \times V_{DDQ}$; however, V_{REFDQ} may be $\geq V_{DDQ}$ provided that $V_{REFDQ} \leq 300mV$.

NOTE 4 Storage Temperature is the case surface temperature on the center/top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.

AC/DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

Recommended DC Operating Conditions

Symbol	Voltage			DRAM	Unit
	Min	Typ	Max		
V_{DD1}	1.70	1.80	1.95	Core Power1	V
V_{DD2}	1.14	1.20	1.30	Core Power2	V
V_{DDCA}	1.14	1.20	1.30	Input Buffer Power	V
V_{DDQ}	1.14	1.20	1.30	I/O Buffer Power	V

NOTE 1 V_{DD1} uses significantly less current than V_{DD2}.

NOTE 2 The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 1MHz at the DRAM package ball.

Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current	I_L	-2	2	uA	1, 2
V_{REF} supply leakage current	I_{VREF}	-1	1	uA	3, 4

NOTE 1 For CA, CKE, $\overline{CS}$, CK, $\overline{CK}$. Any input $0V \le V_{IN} \le V_{DDCA}$ (All other pins not under test = 0V)

NOTE 2 Although DM is for input only, the DM leakage shall match the DQ and DQS/$\overline{DQS}$ output leakage specification.

NOTE 3 The minimum limit requirement is for testing purposes. The leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.

NOTE 4 $V_{REFDQ} = V_{DDQ}/2$ or $V_{REFCA} = V_{DDCA}/2$. (All other pins not under test = 0V)

Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	-30	85	°C
Elevated		85	105	

NOTE 1 Operating Temperature is the case surface temperature on the center-top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 2 Some applications require operation of LPDDR3 in the maximum temperature conditions in the Elevated Temperature Range between 85°C and 105°C case temperature. For LPDDR3 devices, derating may be necessary to operate in this range. See MR4.

NOTE 3 Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Elevated Temperature Ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

AC/DC Input Level

AC and DC Logic Input Levels for Single-Ended Signals

Single-Ended AC and DC Input Levels for CA and $\overline{CS}$ Inputs

Symbol	Parameter	1333/1600		1866		Unit	Notes
		Min	Max	Min	Max		
V_{IHCA}(AC)	AC input logic high	V_{Ref} + 0.150	Note 2	V_{Ref} + 0.135	Note 2	V	1, 2
V_{ILCA}(AC)	AC input logic low	Note 2	V_{Ref} - 0.150	Note 2	V_{Ref} - 0.135	V	1, 2
V_{IHCA}(DC)	DC input logic high	V_{Ref} + 0.100	V_{DDCA}	V_{Ref} + 0.100	V_{DDCA}	V	1
V_{ILCA}(DC)	DC input logic low	V_{SS}	V_{Ref} - 0.100	V_{SS}	V_{Ref} - 0.100	V	1
V_{RefCA}(DC)	Reference Voltage for CA and $\overline{CS}$ inputs	0.49 * V_{DDCA}	0.51 * V_{DDCA}	0.49 * V_{DDCA}	0.51 * V_{DDCA}	V	3, 4

NOTE 1 For CA and $\overline{CS}$ input only pins. $V_{Ref} = V_{RefCA(DC)}$.

NOTE 2 Overshoot and Undershoot Specifications.

NOTE 3 The ac peak noise on V_{RefCA} may not allow V_{RefCA} to deviate from $V_{RefCA(DC)}$ by more than ± 1% V_{DDCA} (for reference: approx. ± 12 mV).

NOTE 4 For reference: approx. $V_{DDCA}/2$ ± 12 mV.

Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE Input High Level	0.65 * V_{DDCA}	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.35 * V_{DDCA}	V	1

NOTE 1 Overshoot and Undershoot Specifications.

Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	1333/1600		1866		Unit	Notes
		Min	Max	Min	Max		
V_{IHDQ}(AC)	AC input logic high	V_{Ref} + 0.150	Note 2	V_{Ref} + 0.135	Note 2	V	1, 2, 5
V_{ILDQ}(AC)	AC input logic low	Note 2	V_{Ref} - 0.150	Note 2	V_{Ref} - 0.135	V	1, 2, 5
V_{IHDQ}(DC)	DC input logic high	V_{Ref} + 0.100	V_{DDQ}	V_{Ref} + 0.100	V_{DDQ}	V	1
V_{ILDQ}(DC)	DC input logic low	V_{SS}	V_{Ref} - 0.100	V_{SS}	V_{Ref} - 0.100	V	1
V_{RefDQ}(DC) (DQ ODT disabled)	Reference Voltage for DQ, DM inputs	0.49 * V_{DDQ}	0.51 * V_{DDQ}	0.49 * V_{DDQ}	0.51 * V_{DDQ}	V	3, 4
V_{RefDQ}(DC) (DQ ODT enabled)	Reference Voltage for DQ, DM inputs	V_{ODTR}/2 - 0.01 * V_{DDQ}	V_{ODTR}/2 + 0.01 * V_{DDQ}	V_{ODTR}/2 - 0.01 * V_{DDQ}	V_{ODTR}/2 + 0.01 * V_{DDQ}	V	3, 5, 6

NOTE 1 For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

NOTE 2 Overshoot and Undershoot Specifications.

NOTE 3 The ac peak noise on V_{RefDQ} may not allow V_{RefDQ} to deviate from $V_{RefDQ(DC)}$ by more than ± 1% V_{DDQ} (for reference: approx. ± 12 mV).

NOTE 4 For reference: approx. $V_{DDQ}/2$ ± 12 mV.

NOTE 5 For reference: approx. $V_{ODTR}/2$ ± 12 mV.

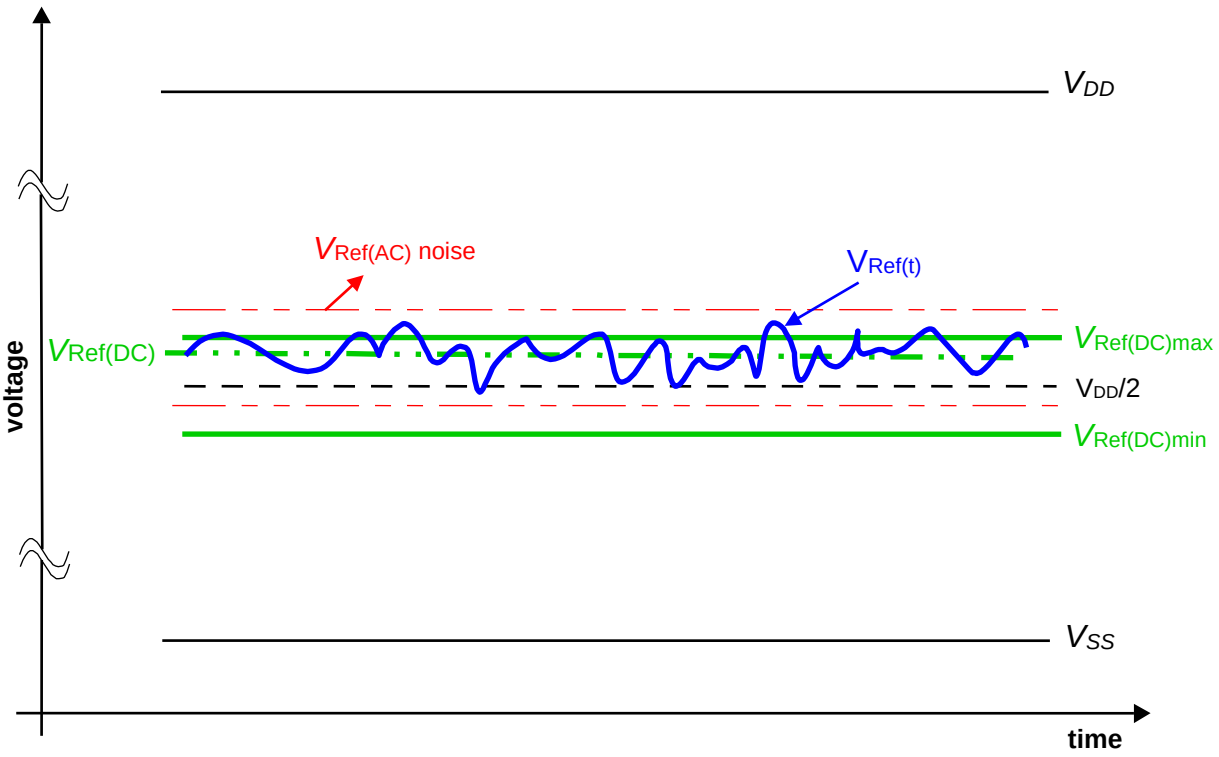
NOTE 6 R_{ON} and R_{ODT} nominal mode register programmed values are used for the calculation of V_{ODTR}. For testing purposes a controller RON value of 50 Ω is used.

$$V_{ODTR} = \frac{2R_{ON} + R_{TT}}{R_{ON} + R_{TT}} \times V_{DDQ}$$

V_{REF} Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{RefCA} and V_{RefDQ} are illustrated below. It shows a valid reference voltage V_{Ref}(t) as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise). V_{DD} stands for V_{DDCA} for V_{RefCA} and V_{DDQ} for V_{RefDQ}. $V_{REF(DC)}$ is the linear average of V_{Ref}(t) over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of V_{DDQ} or V_{DDCA} also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements. Furthermore V_{Ref}(t) may temporarily deviate from $V_{REF(DC)}$ by no more than ± 1% V_{DD}. V_{Ref}(t) cannot track noise on V_{DDQ} or V_{DDCA} if this would send V_{Ref} outside these specifications.

V_{REF} DC Tolerance and V_{REF} AC Noise Limits



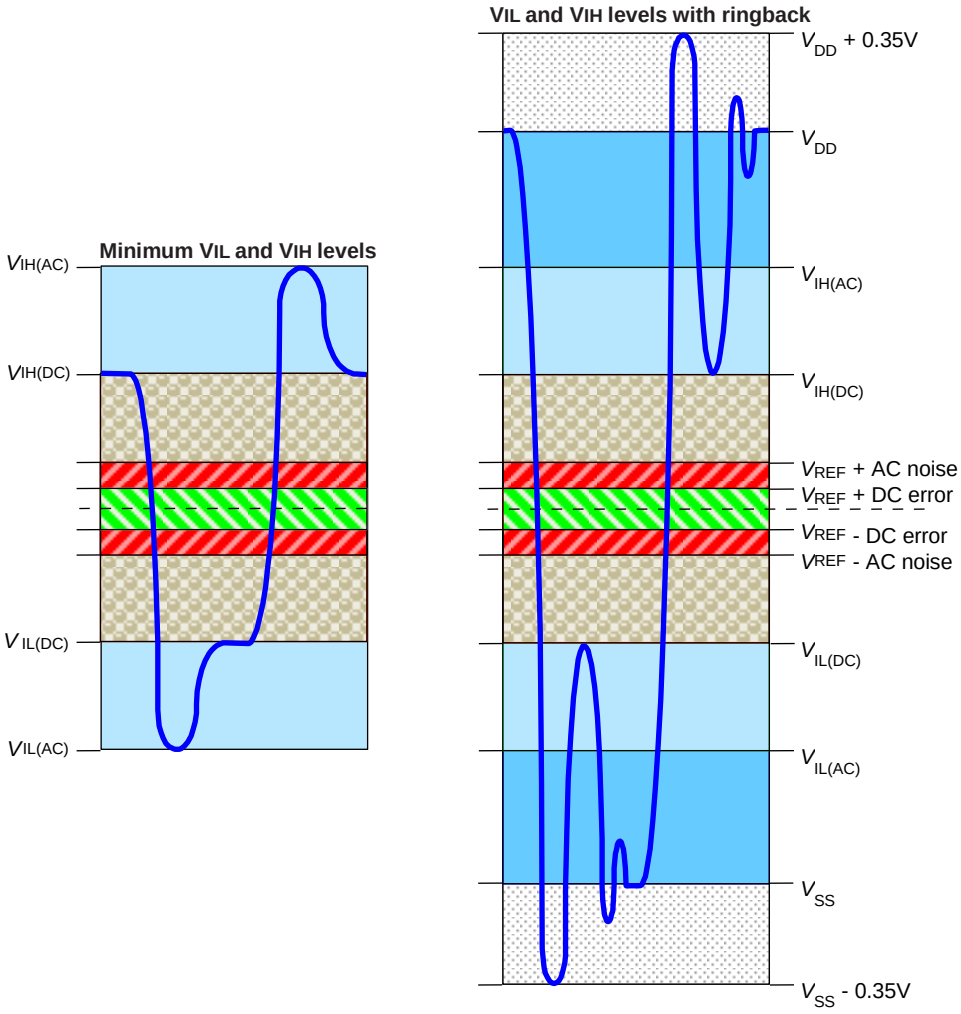
The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on V_{Ref}. "V_{Ref} " shall be understood as $V_{REF(DC)}$ above.

This clarifies that dc-variations of VRef affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the LPDDR3 setup/hold specification and derating values need to include time and voltage associated with VRef ac-noise. Timing and voltage effects due to ac-noise on VRef up to the specified limit (+/-1% of VDD) are included in LPDDR3 timings and their associated deratings.

Input Signal

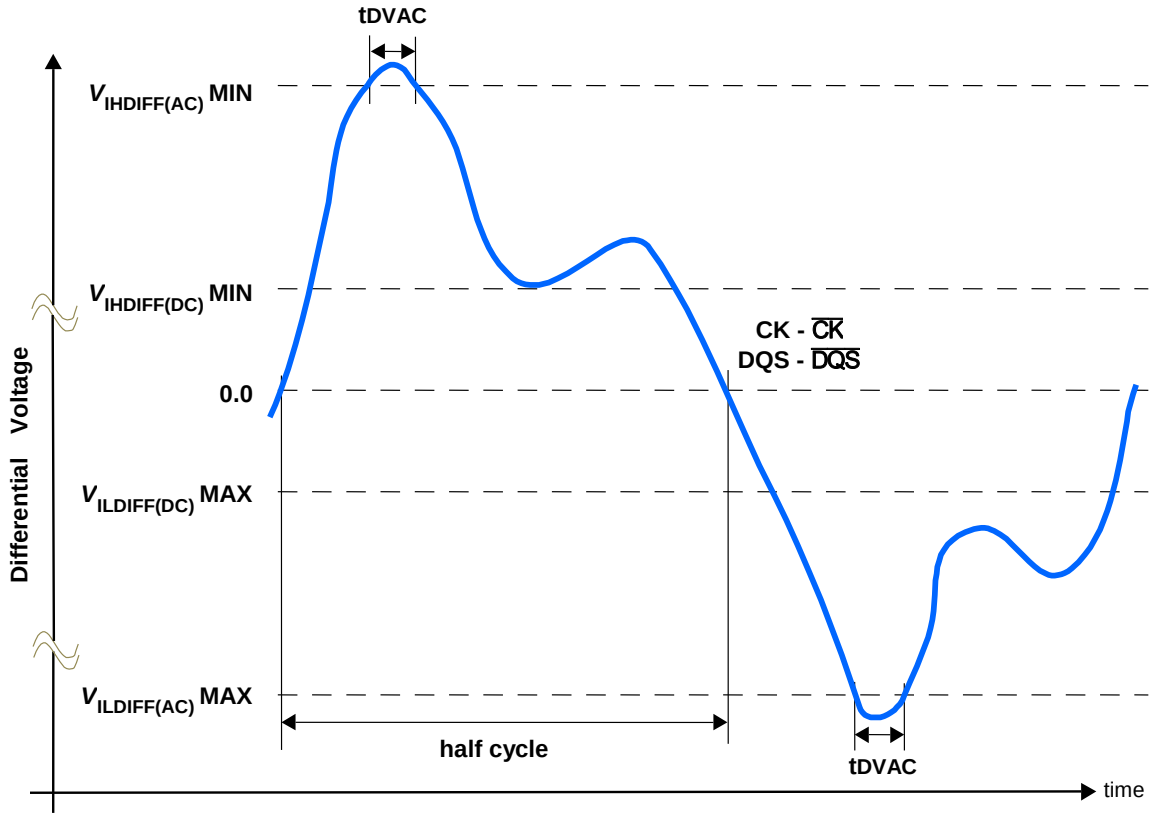
LPDDR3-1866 to LPDDR3-1333 Input Signal



NOTE 1 Numbers reflect typical values.
NOTE 2 For CA[9:0], CK, $\overline{CK}$, and $\overline{CS}$, VDD stands for VDDCA. For DQ, DM, DQS, $\overline{DQS}$, and ODT, VDD stands for VDDQ.
NOTE 3 For CA[9:0], CK, $\overline{CK}$, and $\overline{CS}$, VSS stands for VSS. For DQ, DM, DQS, $\overline{DQS}$, and ODT, VSS stands for VSS.

AC and DC Logic Input Levels for Differential Signals

Differential AC Swing Time and "time above ac-level" tDVAC



Differential swing requirements for clock (CK - $\overline{CK}$) and strobe (DQS - $\overline{DQS}$)

For CK and $\overline{CK}$, VREF = VREFCA(DC); For DQS and $\overline{DQS}$, VREF = VREFDQ(DC)

Differential AC and DC Input Levels

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
$V_{IHdiff(dc)}$	Differential input high	2 x (V_{IH}(dc) - V_{Ref})	Note 3	V	1
$V_{ILdiff(dc)}$	Differential input low	Note 3	2 x (V_{IL}(dc) - V_{Ref})	V	1
$V_{IHdiff(ac)}$	Differential input high ac	2 x (V_{IH}(ac) - V_{Ref})	Note 3	V	2
$V_{ILdiff(ac)}$	Differential input low ac	Note 3	2 x (V_{IL}(ac) - V_{Ref})	V	2

NOTE 1 Used to define a differential signal slew-rate. For CK - $\overline{CK}$ use $V_{IH}/V_{IL(dc)}$ of CA and V_{REFCA}; for DQS - $\overline{DQS}$, use $V_{IH}/V_{IL(dc)}$ of DQs and V_{REFDQ}; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.

NOTE 2 For CK - $\overline{CK}$ use $V_{IH}/V_{IL(ac)}$ of CA and V_{REFCA}; for DQS - $\overline{DQS}$, use $V_{IH}/V_{IL(ac)}$ of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

NOTE 3 These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, and $\overline{DQS}$ need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)min}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Overshoot and Undershoot Specifications.

NOTE 4 For CK and $\overline{CK}$, $V_{Ref} = V_{RefCA(DC)}$. For DQS and $\overline{DQS}$, $V_{Ref} = V_{RefDQ(DC)}$.

Allowed time before ringback tDVAC for Strobe (DQS - $\overline{DQS}$)

Slew Rate [V/ns]	t_{DVAC} [ps] @ $\|V_{IH/Ldiff(ac)}\|$ = 270mV 1866Mbps		t_{DVAC} [ps] @ $\|V_{IH/Ldiff(ac)}\|$ = 300mV 1600Mbps		t_{DVAC} [ps] @ $\|V_{IH/Ldiff(ac)}\|$ = 300mV 1333Mbps	
	min	max	min	max	min	max
> 8.0	40	—	48	—	58	—
8.0	40	—	48	—	58	—
7.0	39	—	46	—	56	—
6.0	36	—	43	—	53	—
5.0	33	—	40	—	50	—
4.0	29	—	35	—	45	—
3.0	21	—	27	—	37	—
< 3.0	21	—	27	—	37	—

Allowed time before ringback tDVAC for Clock (CK - $\overline{CK}$)

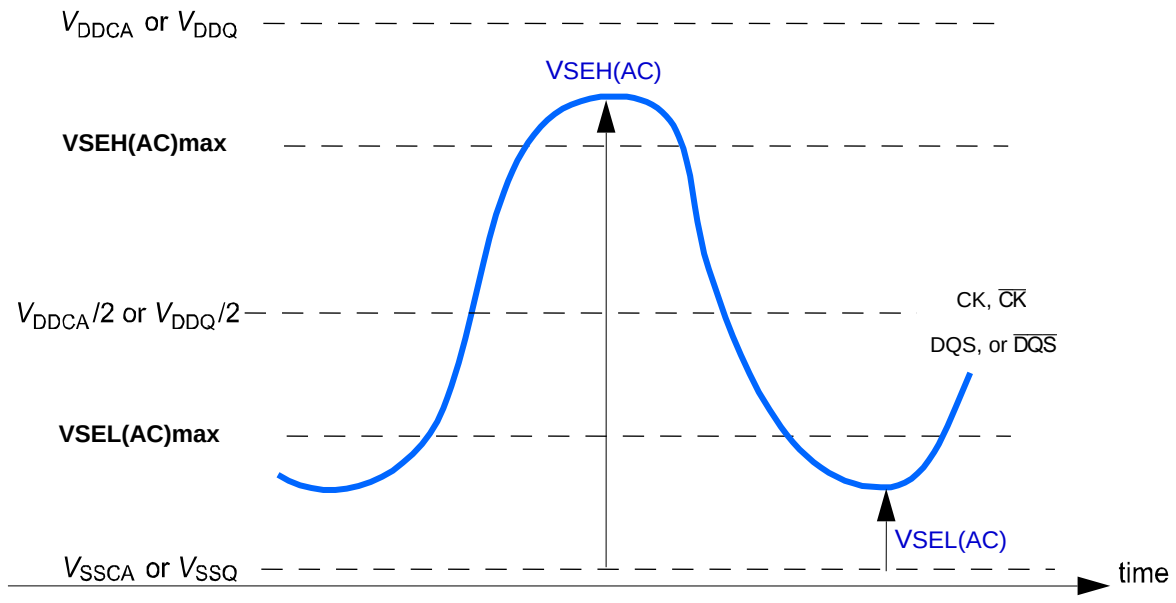
Slew Rate [V/ns]	t_{DVAC} [ps] @ $\|V_{IH/Ldiff(ac)}\|$ = 270mV 1866Mbps		t_{DVAC} [ps] @ $\|V_{IH/Ldiff(ac)}\|$ = 300mV 1600Mbps		t_{DVAC} [ps] @ $\|V_{IH/Ldiff(ac)}\|$ = 300mV 1333Mbps	
	min	max	min	max	min	max
> 8.0	40	—	48	—	58	—
8.0	40	—	48	—	58	—
7.0	39	—	46	—	56	—
6.0	36	—	43	—	53	—
5.0	33	—	40	—	50	—
4.0	29	—	35	—	45	—
3.0	21	—	27	—	37	—
< 3.0	21	—	27	—	37	—

Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, $\overline{CK}$, or $\overline{DQS}$) has also to comply with certain requirements for single-ended signals. The applicable AC levels for CA and DQ differ by speed bin.

- CK and $\overline{CK}$ shall meet $V_{SEH(ac)min}$ / $V_{SEL(ac)max}$ in every half-cycle.
- DQS, $\overline{DQS}$ shall meet $V_{SEH(ac)min}$ / $V_{SEL(ac)max}$ in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.



Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to $V_{DDQ}/2$ for DQS, $\overline{DQS}$ and $V_{DDCA}/2$ for CK, $\overline{CK}$; this is nominally the same.

The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL(ac)max}$, $V_{SEH(ac)min}$ has no bearing on timing, but adds a restriction on the common mode characteristics of these signals (See tables: Single-Ended AC and DC Input Levels for CA and $\overline{CS}$ Inputs; Single-Ended AC and DC Input Levels for DQ and DM).

Single-ended levels for CK, DQS, $\overline{CK}$, $\overline{DQS}$

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
*V*SEH(AC150)	Single-ended high-level for strobes	(V_{DDQ} / 2) + 0.150	Note 3	V	1, 2
	Single-ended high-level for CK, $\overline{CK}$	(V_{DDCA} / 2) + 0.150	Note 3	V	1, 2
*V*SEL(AC150)	Single-ended low-level for strobes	Note 3	(V_{DDQ} / 2) - 0.150	V	1, 2
	Single-ended low-level for CK, $\overline{CK}$	Note 3	(V_{DDCA} / 2) - 0.150	V	1, 2
*V*SEH(AC135)	Single-ended high-level for strobes	(V_{DDQ} / 2) + 0.135	Note 3	V	1, 2
	Single-ended high-level for CK, $\overline{CK}$	(V_{DDCA} / 2) + 0.135	Note 3	V	1, 2
*V*SEL(AC135)	Single-ended low-level for strobes	Note 3	(V_{DDQ} / 2) - 0.135	V	1, 2
	Single-ended low-level for CK, $\overline{CK}$	Note 3	(V_{DDCA} / 2) - 0.135	V	1, 2

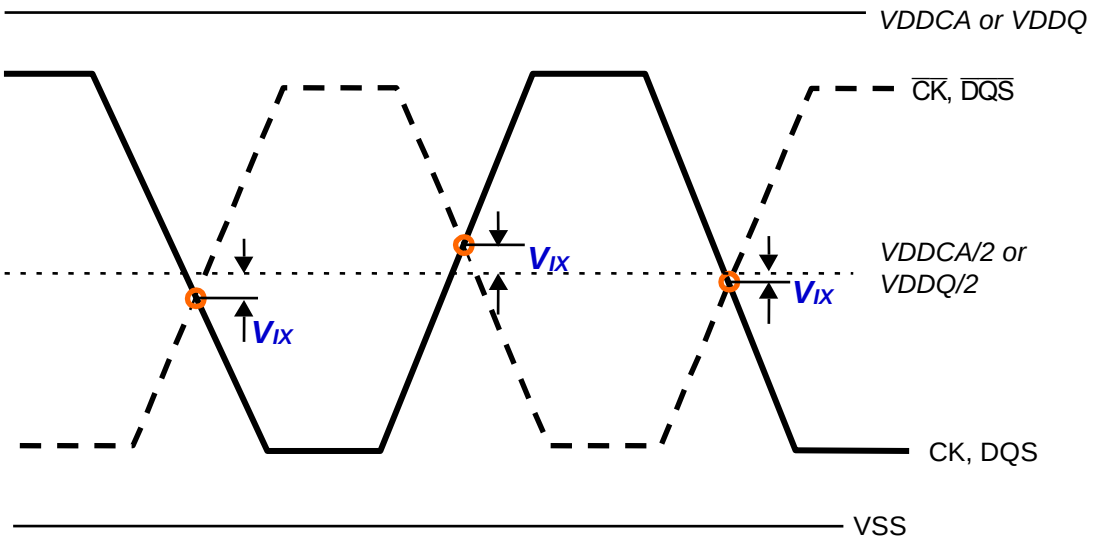
NOTE 1 For CK, $\overline{CK}$ use $V_{SEH}/V_{SEL(ac)}$ of CA; for strobes (DQS0, $\overline{DQS0}$, DQS1, $\overline{DQS1}$, DQS2, $\overline{DQS2}$, DQS3, $\overline{DQS3}$) use $V_{IH}/V_{IL(ac)}$ of DQs.

NOTE 2 $V_{IH(ac)}/V_{IL(ac)}$ for DQs is based on V_{REFDQ}; $V_{SEH(ac)}/V_{SEL(ac)}$ for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here

NOTE 3 These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS0, $\overline{DQS0}$, DQS1, $\overline{DQS1}$, DQS2, $\overline{DQS2}$, DQS3, $\overline{DQS3}$ need to be within the respective limits ($V_{IH(dc)\ max}$, $V_{IL(dc)min}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Overshoot and Undershoot Specifications.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of V_{DD} and V_{SS}.



Symbol	Parameter	Value		Unit	Notes
		Min	Max		
VIXCA	Differential Input Cross Point Voltage relative to V_{DDCA}/2 for CK, $\overline{CK}$	- 120	120	mV	1,2
VIXDQ	Differential Input Cross Point Voltage relative to V_{DDQ}/2 for DQS, $\overline{DQS}$	- 120	120	mV	1,2

NOTE 1 The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.

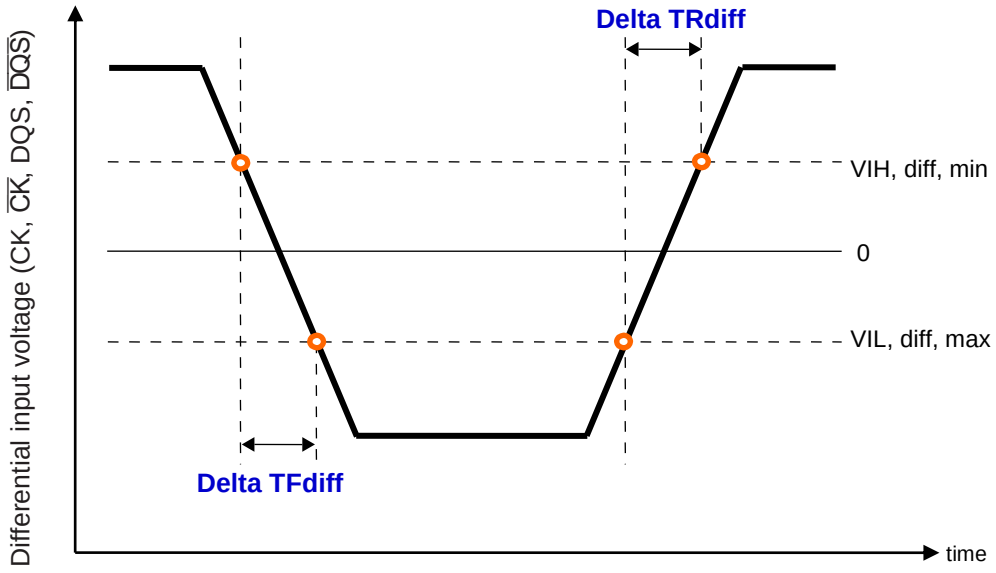
NOTE 2 For CK and $\overline{CK}$, $V_{Ref} = V_{RefCA(DC)}$. For DQS and $\overline{DQS}$, $V_{Ref} = V_{RefDQ(DC)}$.

Slew Rate Definitions for Differential Input Signals

Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK - $\overline{CK}$ and DQS - $\overline{DQS}$).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTRdiff
Differential input slew rate for falling edge (CK - $\overline{CK}$ and DQS - $\overline{DQS}$).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTFdiff
NOTE 1 The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be linear between these thresholds.			

Differential Input Slew Rate Definition for CK, $\overline{CK}$, DQS, and $\overline{DQS}$



AC and DC Output Measurement Levels

Single Ended AC and DC Output Levels

Symbol	Parameter			Value	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)			0.9 x V_{DDQ}	V	1
$V_{OL(DC)}$	ODT disabled	DC output low measurement level (for IV curve linearity)		0.1 x V_{DDQ}	V	2
$V_{OL(DC)}$	ODT enabled			V_{DDQ} x [0.1 + 0.9 x (R_{ON} / (R_{TT} + R_{ON}))]	V	3
$V_{OH(AC)}$	AC output high measurement level (for output slew rate)			V_{REFDQ} + 0.12	V	
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)			V_{REFDQ} - 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS, $\overline{DQS}$) (DQ, DQS, $\overline{DQS}$ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}		Min	-5	uA	
			Max	5	uA	

NOTE 1 I_{OH} = -0.1mA.
NOTE 2 I_{OL} = 0.1mA.
NOTE 3 The minimum value is derived when using RTT,min and RON,max (±30% uncalibrated, ±15% calibrated).

Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.20 x V_{DDQ}	V	1
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.20 x V_{DDQ}	V	2

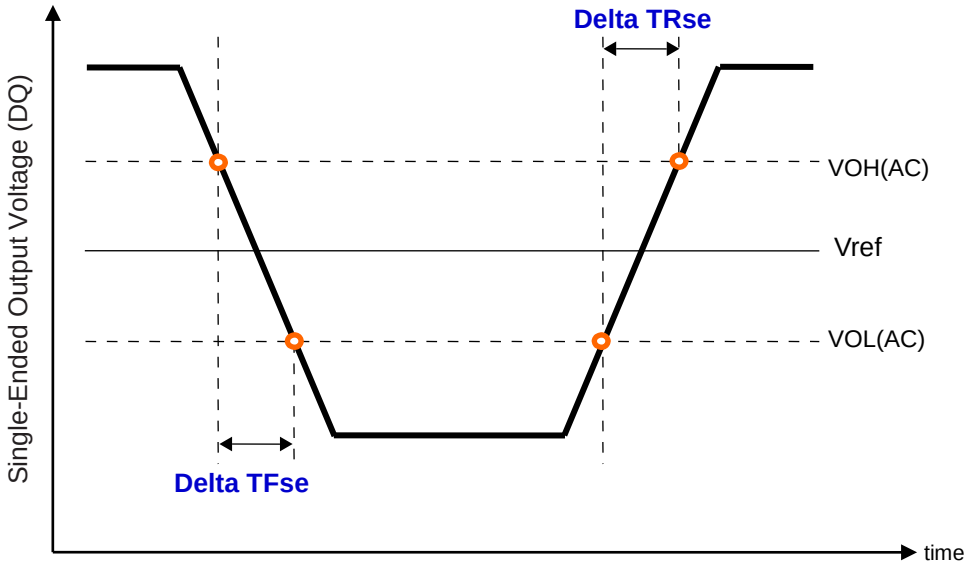
NOTE 1 I_{OH} = -0.1mA.
NOTE 2 I_{OL} = 0.1mA

Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals.

Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTFse
NOTE Output slew rate is verified, and may not be subject to production test.			



Single-ended Output Slew Rate

Parameter	Symbol	Value		Units
		Min[1]	Max[2]	
Single-ended Output Slew Rate (RON = 40Ω +/- 30%)	SRQse	1.5	4.0	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	

Description: SR: Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output); se: Single-ended Signals

NOTE 1 Measured with output reference load.

NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

NOTE 3 The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.

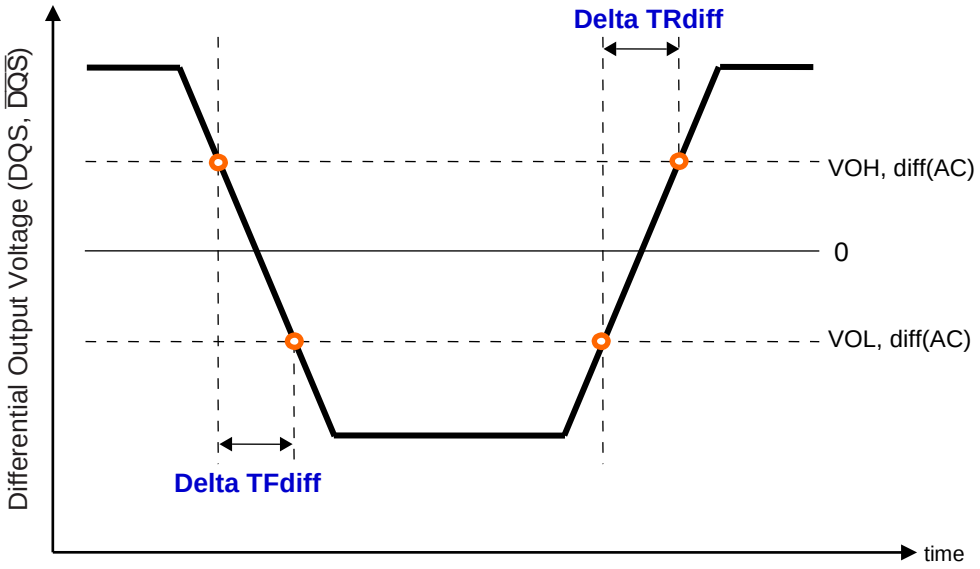
NOTE 4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals.

Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / DeltaTFdiff
NOTE 1 Output slew rate is verified, and may not be subject to production test.			



Differential Output Slew Rate

Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate (R_{ON} = 40Ω +/- 30%)	SRQdiff	3.0	8.0	V/ns

Description: SR: Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output); diff: Differential Signals

NOTE 1 Measured with output reference load.

NOTE 2 The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.

NOTE 3 Slew rates are measured under normal SSO conditions, with 50% of DQ signals per data byte switching.

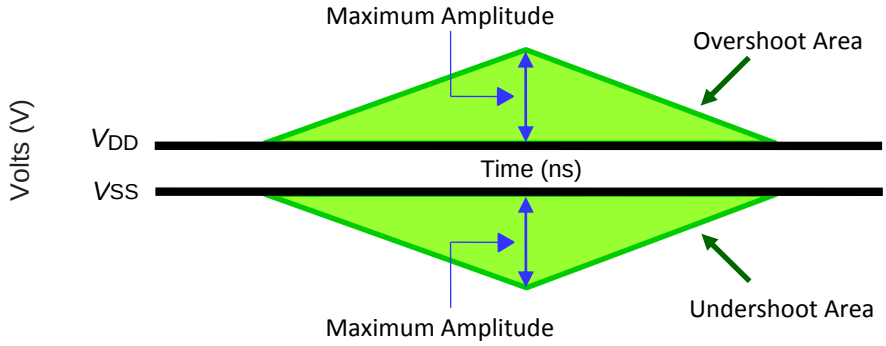
Overshoot and Undershoot Specifications

AC Overshoot/Undershoot Specification

Parameter		1333	1600/1866	Units
Maximum peak amplitude allowed for overshoot area.	Max	0.35		V
Maximum peak amplitude allowed for undershoot area.	Max	0.35		V
Maximum area above VDD.	Max	0.12	0.10	V-ns
Maximum area below VSS.	Max	0.12	0.10	V-ns

NOTE 1 V_{DD} stands for V_{DDCA} for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. V_{DD} stands for V_{DDQ} for DQ, DM, ODT, DQS, and $\overline{DQS}$.
NOTE 2 V_{SS} stands for V_{SS} for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. V_{SS} stands for V_{SS} for DQ, DM, ODT, DQS, and $\overline{DQS}$.
NOTE 3 Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
NOTE 4 Maximum area values are referenced from maximm operating V_{DD} and V_{SS} values.

Overshoot and Undershoot Definition

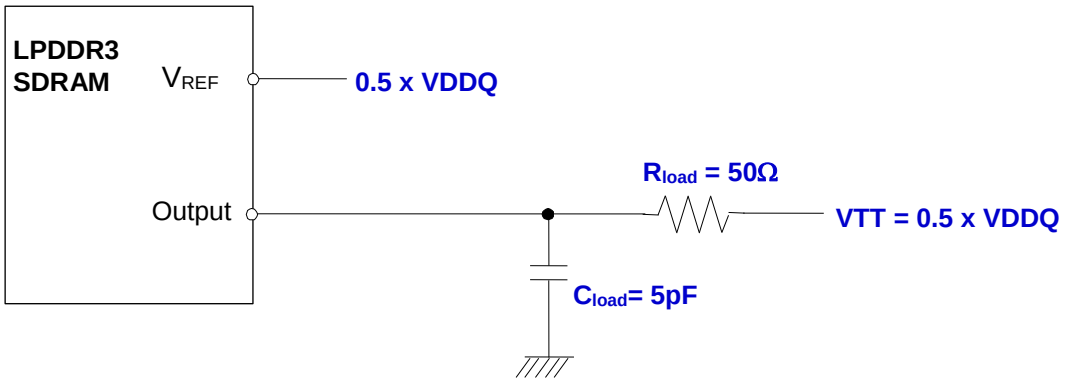


NOTE 1 VDD = VDDCA for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. VDD = VDDQ for DQ, DM, DQS, $\overline{DQS}$, and ODT.
NOTE 2 VSS = VSS for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. VSS = VSS for DQ, DM, DQS, $\overline{DQS}$, and ODT.
NOTE 3 Absolute maximum requirements apply.
NOTE 4 Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
NOTE 5 Maximum area values are referenced from maximum operating V_{DD} and V_{SS} values.

Output buffer characteristics

HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



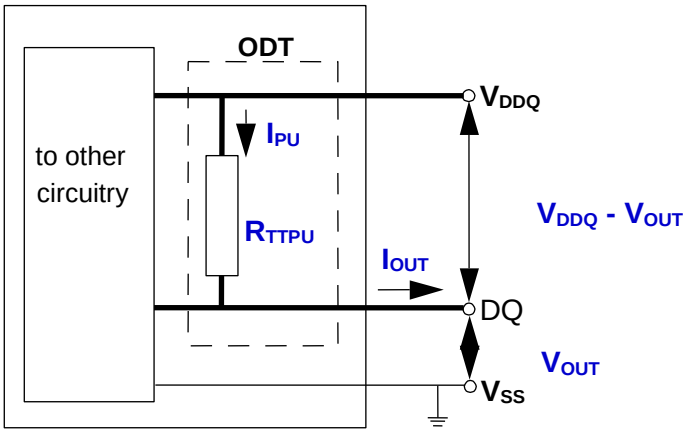
NOTE 1 All output timing parameter values (tDQSCK, tDQSQ, tHZ, tRPRE, etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

ODT Levels and I-V Characteristics

On-Die Termination effective resistance, R_{TT}, is defined by mode register MR11[1:0]. ODT is applied to the DQ, DM, and DQS/$\overline{\text{DQS}}$ pins. A functional representation of the on-die termination is shown in the figure below.

R_{TT} is defined by the following formula:

$$R_{TTPU} = (V_{DDQ} - V_{Out}) / | I_{Out} |$$



Input/output capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input capacitance, CK and $\overline{CK}$	C_{CK}	0.5	1.2	pF	1,2
Input capacitance delta, CK and $\overline{CK}$	C_{DCK}	0	0.15	pF	1,2,3
Input capacitance, all other input-only pins	C_I	0.5	1.1	pF	1,2,4
Input capacitance delta, all other input-only pins	C_{DI}	-0.20	0.20	pF	1,2,5
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	C_{IO}	1.0	1.8	pF	1,2,6,7
Input/output capacitance delta, DQS, $\overline{DQS}$	C_{DDQS}	0	0.2	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	C_{DIO}	-0.25	0.25	pF	1,2,7,9
Input/output capacitance ZQ Pin	C_{ZQ}	0	2.0	pF	1,2

(T_{OPER} ;V_{DDQ} = 1.14-1.3V; V_{DDCA} = 1.14-1.3V; V_{DD1} = 1.7-1.95V, V_{DD2} = 1.14-1.3V)

NOTE 1 This parameter applies to die device only (does not include package capacitance).

NOTE 2 This parameter is not subject to production test. It is verified. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SS}, V_{SS} applied and all other pins floating.

NOTE 3 Absolute value of C_{CK} - $C_{\overline{CK}}$.

NOTE 4 C_I applies to $\overline{CS}$, CKE, CA0-CA9, ODT.

NOTE 5 $C_{DI} = C_I - 0.5 * (C_{CK} + C_{\overline{CK}})$

NOTE 6 DM loading matches DQ and DQS.

NOTE 7 MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ω typical)

NOTE 8 Absolute value of C_{DQS} and $C_{\overline{DQS}}$.

NOTE 9 $C_{DIO} = C_{IO} - 0.5 * (C_{DQS} + C_{\overline{DQS}})$ in byte-lane.

IDD Specification Parameters and Test Conditions

I_{DD} Measurement Conditions

The following definitions are used within the I_{DD} measurement tables unless stated otherwise:

LOW: *V*IN ≤ *V*IL(DC) MAX

HIGH: *V*IN ≥ *V*IH(DC) MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See following 3 tables.

Definition of Switching for CA Input Signals

Switching for CA								
	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)
Cycle	N		N+1		N+2		N+3	
$\overline{CS}$	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE 1 $\overline{CS}$ must always be driven HIGH.

NOTE 2 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.

NOTE 3 The above pattern (N, N+1, N+2, N+3...) is used continuously during I_{DD} measurement for I_{DD} values that require SWITCHING on the CA bus.

Definition of Switching for IDD4R

Clock	CKE	$\overline{CS}$	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	LLL	LLLLLLL	L
Rising	H	H	N + 2	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 2	NOP	LLL	LLLLLLL	H
Rising	H	H	N + 3	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 3	NOP	HLH	HLHLLHL	L
Rising	H	L	N + 4	Read_Rising	HLH	HLHLLHL	H
Falling	H	L	N + 4	Read_Falling	LHH	HHHHHHH	H
Rising	H	H	N + 5	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 5	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 6	NOP	HHH	HHHHHHH	L
Falling	H	H	N + 6	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 7	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 7	NOP	HLH	LHLHLHL	L

NOTE 1 Data strobe (DQS) is changing between HIGH and LOW every clock cycle.

NOTE 2 The above pattern (N, N+1...) is used continuously during I_{DD} measurement for I_{DD4R}.

Definition of Switching for IDD4W

Clock	CKE	$\overline{CS}$	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQ
Rising	H	L	N	Write_Rising	HLL	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	LLL	LLLLLLL	L
Rising	H	H	N + 2	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 2	NOP	LLL	LLLLLLL	H
Rising	H	H	N + 3	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 3	NOP	HLL	HLHLLHL	L
Rising	H	L	N + 4	Write_Rising	HLL	HLHLLHL	H
Falling	H	L	N + 4	Write_Falling	LHH	HHHHHHH	H
Rising	H	H	N + 5	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 5	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 6	NOP	HHH	HHHHHHH	L
Falling	H	H	N + 6	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 7	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 7	NOP	HLL	LHLHLHL	L

NOTE 1 Data strobe (DQS) is changing between HIGH and LOW every clock cycle.

NOTE 2 Data masking (DM) must always be driven LOW.

NOTE 3 The above pattern (N, N+1...) is used continuously during I_{DD} measurement for I_{DD4W}.

IDD Specifications

I_{DD} values are for the entire operating voltage range, and all of them are for the entire standard range.

I_{DD} Specification Parameters and Operating Conditions

Notes 1, 2, 3 apply for all values.

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: tCK =tCK (MIN); tRC = tRC (MIN); CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD01}	V_{DD1}	
	I_{DD02}	V_{DD2}	
	I_{DD0in}	V_{DDCA}, V_{DDQ}	4
Idle power-down standby current: tCK = tCK (MIN); CKE is LOW; $\overline{CS}$ is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2P1}	V_{DD1}	
	I_{DD2P2}	V_{DD2}	
	$I_{DD2P,in}$	V_{DDCA}, V_{DDQ}	4
Idle power-down standby current with clock stop: CK= LOW, $\overline{CK}$ = HIGH; CKE is LOW; $\overline{CS}$ is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2PS1}	V_{DD1}	
	I_{DD2PS2}	V_{DD2}	
	$I_{DD2PS,in}$	V_{DDCA}, V_{DDQ}	4
Idle non-power-down standby current: tCK = tCK (MIN); CKE is HIGH; $\overline{CS}$ is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2N1}	V_{DD1}	
	I_{DD2N2}	V_{DD2}	
	$I_{DD2N,in}$	V_{DDCA}, V_{DDQ}	4
Idle non-power-down standby current with clock stopped: CK = LOW; $\overline{CK}$ = HIGH; CKE is HIGH; $\overline{CS}$ is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2NS1}	V_{DD1}	
	I_{DD2NS2}	V_{DD2}	
	$I_{DD2NS,in}$	V_{DDCA}, V_{DDQ}	4
Active power-down standby current: tCK = tCK (MIN); CKE is LOW; $\overline{CS}$ is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3P1}	V_{DD1}	
	I_{DD3P2}	V_{DD2}	
	$I_{DD3P,in}$	V_{DDCA}, V_{DDQ}	4
Active power-down standby current with clock stop: CK = LOW, $\overline{CK}$ = HIGH; CKE is LOW; $\overline{CS}$ is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable;ODT is disabled	I_{DD3PS1}	V_{DD1}	
	I_{DD3PS2}	V_{DD2}	
	$I_{DD3PS,in}$	V_{DDCA}, V_{DDQ}	4
Active non-power-down standby current: tCK = tCK (MIN); CKE is HIGH; $\overline{CS}$ is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3N1}	V_{DD1}	
	I_{DD3N2}	V_{DD2}	
	$I_{DD3N,in}$	V_{DDCA}, V_{DDQ}	4
Active non-power-down standby current with clock stopped: CK = LOW, $\overline{CK}$ = HIGH; CKE is HIGH; $\overline{CS}$ is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3NS1}	V_{DD1}	
	I_{DD3NS2}	V_{DD2}	
	$I_{DD3NS,in}$	V_{DDCA}, V_{DDQ}	4
Operating burst READ current: tCK = tCK (MIN); $\overline{CS}$ is HIGH between valid commands; One bank is active; BL = 8; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4R1}	V_{DD1}	
	I_{DD4R2}	V_{DD2}	
	$I_{DD4R,in}$	V_{DDCA}	
	I_{DD4RQ}	V_{DDQ}	5
Operating burst WRITE current: tCK = tCK (MIN); $\overline{CS}$ is HIGH between valid commands; One bank is active; BL = 8; WL = WL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4W1}	V_{DD1}	
	I_{DD4W2}	V_{DD2}	
	$I_{DD4W,in}$	V_{DDCA}, V_{DDQ}	4

Parameter/Condition	Symbol	Power Supply	Notes
All-bank REFRESH burst current: tCK = tCK (MIN); CKE is HIGH between valid commands; tRC = tRFCab (MIN); Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD51}	V_{DD1}	
	I_{DD52}	V_{DD2}	
	I_{DD5IN}	V_{DDCA}, V_{DDQ}	4
All-bank REFRESH average current: tCK = tCK (MIN); CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5AB1}	V_{DD1}	
	I_{DD5AB2}	V_{DD2}	
	$I_{DD5AB,in}$	V_{DDCA}, V_{DDQ}	4
Per-bank REFRESH average current: tCK = tCK (MIN); CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5PB1}	V_{DD1}	
	I_{DD5PB2}	V_{DD2}	
	$I_{DD5PB,in}$	V_{DDCA}, V_{DDQ}	4
Self refresh current (TC ≦ +85˚C): CK = LOW, $\overline{CK}$ = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate; ODT is disabled	I_{DD61}	V_{DD1}	6, 7
	I_{DD62}	V_{DD2}	6, 7
	I_{DD6IN}	V_{DDCA}, V_{DDQ}	4,7

NOTE 1 Published IDD values are the maximum of the distribution of the arithmetic mean and are measured at 85℃.

NOTE 2 ODT disabled: MR11[2:0] = 000B.

NOTE 3 I_{DD} current specifications are tested after the device is properly initialized.

NOTE 4 Measured currents are the summation of V_{DDQ} and V_{DDCA}.

NOTE 5 Guaranteed by design with output load = 5 pF and R_{ON} = 40 ohm.

NOTE 6 The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the elevated temperature range.

NOTE 7 This is the general definition that applies to full-array SELF REFRESH.

NOTE 8 Published IDD values of DDP can support x32 and x16 I/O configuration.

NOTE 9 IDD will be derated (increased) when above 85℃.

I_{DD6} Partial Array Self-Refresh Current

Parameter		Unit
I_{DD6} Partial Array Self-Refresh Current	Full Array	µA
	1/2 Array	µA
	1/4 Array	µA
	1/8 Array	µA

NOTE 1 I_{DD6} currents are measured using bank-masking only.

NOTE 2 I_{DD} values published are the maximum of the distribution of the arithmetic mean.

IDD Specifications

Parameter Condition	Symbol	Power Supply	1866		Unit
			SDP	DDP	
Operating one bank active-precharge current	I_{DD01}	V_{DD1}	TBD	TBD	mA
	I_{DD02}	V_{DD2}	TBD	TBD	
	I_{DD0in}	V_{DDCA}, V_{DDQ}	TBD	TBD	
Idle power-down standby current	I_{DD2P1}	V_{DD1}	TBD	TBD	µA
	I_{DD2P2}	V_{DD2}	TBD	TBD	
	$I_{DD2P,in}$	V_{DDCA}, V_{DDQ}	TBD	TBD	
Idle power-down standby current with clock stop	I_{DD2PS1}	V_{DD1}	TBD	TBD	µA
	I_{DD2PS2}	V_{DD2}	TBD	TBD	
	$I_{DD2PS,in}$	V_{DDCA}, V_{DDQ}	TBD	TBD	
Idle non-power-down standby current	I_{DD2N1}	V_{DD1}	TBD	TBD	mA
	I_{DD2N2}	V_{DD2}	TBD	TBD	
	$I_{DD2N,in}$	V_{DDCA}, V_{DDQ}	TBD	TBD	
Idle non-power-down standby current with clock stopped	I_{DD2NS1}	V_{DD1}	TBD	TBD	mA
	I_{DD2NS2}	V_{DD2}	TBD	TBD	
	$I_{DD2NS,in}$	V_{DDCA}, V_{DDQ}	TBD	TBD	
Active power-down standby current	I_{DD3P1}	V_{DD1}	TBD	TBD	µA
	I_{DD3P2}	V_{DD2}	TBD	TBD	µA
	$I_{DD3P,in}$	V_{DDCA}, V_{DDQ}	TBD	TBD	µA
Active power-down standby current with clock stop	I_{DD3PS1}	V_{DD1}	TBD	TBD	µA
	I_{DD3PS2}	V_{DD2}	TBD	TBD	µA
	$I_{DD3PS,in}$	V_{DDCA}, V_{DDQ}	TBD	TBD	µA
Active non-power-down standby current	I_{DD3N1}	V_{DD1}	TBD	TBD	mA
	I_{DD3N2}	V_{DD2}	TBD	TBD	
	$I_{DD3N,in}$	V_{DDCA}, V_{DDQ}	TBD	TBD	
Active non-power-down standby current with clock stopped	I_{DD3NS1}	V_{DD1}	TBD	TBD	mA
	I_{DD3NS2}	V_{DD2}	TBD	TBD	
	$I_{DD3NS,in}$	V_{DDCA}, V_{DDQ}	TBD	TBD	
Operating burst READ current	I_{DD4R1}	V_{DD1}	TBD	TBD	mA
	I_{DD4R2}	V_{DD2}	TBD	TBD	
	$I_{DD4R,in}$	V_{DDCA}	TBD	TBD	
Operating burst WRITE current	I_{DD4W1}	V_{DD1}	TBD	TBD	mA
	I_{DD4W2}	V_{DD2}	TBD	TBD	
	$I_{DD4W,in}$	V_{DDCA}, V_{DDQ}	TBD	TBD	

Parameter Condition	Symbol	Power Supply	1866		Unit
			SDP	DDP	
All-bank REFRESH burst current	I_{DD51}	V_{DD1}	TBD	TBD	mA
	I_{DD52}	V_{DD2}	TBD	TBD	
	I_{DD5IN}	V_{DDCA}, V_{DDQ}	TBD	TBD	
All-bank REFRESH average current	I_{DD5AB1}	V_{DD1}	TBD	TBD	mA
	I_{DD5AB2}	V_{DD2}	TBD	TBD	
	$I_{DD5AB,in}$	V_{DDCA}, V_{DDQ}	TBD	TBD	
Per-bank REFRESH average current	I_{DD5PB1}	V_{DD1}	TBD	TBD	mA
	I_{DD5PB2}	V_{DD2}	TBD	TBD	
	$I_{DD5PB,in}$	V_{DDCA}, V_{DDQ}	TBD	TBD	
Self refresh current (Full Array; TC ≦ +85˚C)	I_{DD61} (full Array)	V_{DD1}	TBD	TBD	µA
	I_{DD62} (full Array)	V_{DD2}	TBD	TBD	
	I_{DD6IN} (full Array)	V_{DDCA}, V_{DDQ}	TBD	TBD	
Self refresh current (1/2 Array; TC ≦ +85˚C)	I_{DD61} (1/2 Array)	V_{DD1}	TBD	TBD	
	I_{DD62} (1/2 Array)	V_{DD2}	TBD	TBD	
	I_{DD6IN} (1/2 Array)	V_{DDCA}, V_{DDQ}	TBD	TBD	
Self refresh current (1/4 Array; TC ≦ +85˚C)	I_{DD61} (1/4 Array)	V_{DD1}	TBD	TBD	
	I_{DD62} (1/4 Array)	V_{DD2}	TBD	TBD	
	I_{DD6IN} (1/4 Array)	V_{DDCA}, V_{DDQ}	TBD	TBD	
Self refresh current (1/8 Array; TC ≦ +85˚C)	I_{DD61} (1/8 Array)	V_{DD1}	TBD	TBD	
	I_{DD62} (1/8 Array)	V_{DD2}	TBD	TBD	
	I_{DD6IN} (1/8 Array)	V_{DDCA}, V_{DDQ}	TBD	TBD	

Electrical Characteristic and AC Timing

Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Definitions and Calculations

Symbol	Description	Calculation	Notes
tCK(avg) and *n*CK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit *tCK(avg)* represents the actual clock average *tCK(avg)* of the input clock under operation. Unit *nCK* represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. *tCK(avg)* can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j\right) / N$ where $N = 200$	
tCK(abs)	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge. t*CK(abs)* is not subject to production test.		
tCH(avg)	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j\right) / (N \times tCK(avg))$ where $N = 200$	
t*CL(avg)*	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j\right) / (N \times tCK(avg))$ where $N = 200$	
tJIT(per)	The single-period jitter defined as the largest deviation of any signal tCK from *tCK(avg).* t*JIT(per)* is not subject to production test.	$t_{JIT(per)} = min/max\ of \left\{t_{CK_i} - t_{CK(avg)}\right\}$ Where $i = 1$ to 200	
tJIT(per),act	The actual clock jitter for a given system.		
tJIT(per),allowed	The specified clock period jitter allowance.		
tJIT(cc)	The absolute difference in clock periods between two consecutive clock cycles. *tJIT(cc)* defines the cycle-to-cycle jitter. t*JIT(cc)* is not subject to production test.	$t_{JIT(cc)} = max\ of \left\{t_{CK_{i+1}} - t_{CK_i}\right\}$	

Symbol	Description	Calculation	Notes
tERR(nper)	The cumulative error across *n* multiple consecutive cycles from *tCK(avg)*.	$t_{ERR(nper)} = \left(\sum_{j=i}^{i+n-1} t_{CK_j}\right) - (n \times t_{CK(avg)})$	
tERR(nper),act	The actual cumulative error over *n* cycles for a given system.		
tERR(nper),allowed	The specified cumulative error allowance over *n* cycles.		
tERR(nper),min	The minimum *tERR(nper)*.	$t_{ERR(nper),min} = (1 + 0.68LN(n)) \times t_{JIT(per),min}$	
tERR(nper),max	The maximum *tERR(nper)*.	$t_{ERR(nper),max} = (1 + 0.68LN(n)) \times t_{JIT(per),max}$	
tJIT(duty)	Defined with tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from *tCH(avg)*. tCL jitter is the largest deviation of any single tCL from *tCL(avg)*.	**tJIT(duty),min = MIN((tCH(abs),min – tCH(avg),min), (tCL(abs),min – tCL(avg),min)) × tCK(avg)** **tJIT(duty),max = MAX((tCH(abs),max – tCH(avg),max), (tCL(abs),max – tCL(avg),max)) × tCK(avg)**	

Notes:

1. Not subject to production testing.
2. Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value.

Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however, it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Symbol	Parameter	Minimum	Unit
tCK(abs)	Absolute clock period	*tCK(avg),min + tJIT(per),min*	*ps*[1]
tCH(abs)	Absolute clock HIGH pulse width	*tCH(avg),min + tJIT(duty)*[2]*,min/ tCK(avg)min*	*tCK(avg)*
tCL(abs)	Absolute clock LOW pulse width	*tCL(avg),min + tJIT(duty)*[2]*,min / tCK(avg)min*	*tCK(avg)*

Notes:

1. *tCK(avg),min* is expressed in ps for this table.
2. *tJIT(duty),min* is a negative value.

Period Clock Jitter

LPDDR3 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter (tJIT(per)) in excess of the values found in the AC timing table. Calculating cycle time derating and clock cycle derating are also described.

Clock Period Jitter Effects on Core Timing Parameters(*t*RCD, *t*RP, *t*RTP, *t*WR, *t*WRA, *t*WTR, *t*RC,*t*RAS, *t*RRD, *t*FAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support tnPARAM = RU[tPARAM / tCK(avg)]. During device operation where clock jitter is outside specification limits, the number of clocks or tCK(avg), may need to be increased based on the values for each core timing parameter.

Cycle Time Derating for Core Timing Parameters

For a given number of clocks (*t*nPARAM), for each core timing parameter, average clock period (*t*CK(avg)) and actual cumulative period error (*t*ERR(*t*nPARAM),act) in excess of the allowed cumulative period error (*t*ERR(*t*nPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter.

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

Clock Cycle Derating for Core Timing Parameters

For a given number of clocks (*t*nPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (*t*JIT(per)).

For a given number of clocks (*t*nPARAM), for each core timing parameter, average clock period (*t*CK(avg)) and actual cumulative period error (*t*ERR(*t*nPARAM),act) in excess of the allowed cumulative period error (*t*ERR(*t*nPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter.

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

Clock Jitter Effects on Command/Address Timing Parameters(*t*ISCA, *t*IHCA, *t*ISCS, *t*IHCS,*t*ISCKE,*t*IHCKE, *t*ISb, *t*IHb, *t*ISCKEb, *t*IHCKEb)

These parameters are measured from a command/address signal (CKE, $\overline{CS}$, CA0 - CA9) transition edge to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

Clock Jitter Effects on READ Timing Parameters

tRPRE

When the device is operated with input clock jitter, tRPRE must be derated by the actual period jitter(tJIT(per),act,max) of the input clock that exceeds the allowed period jitter(tJIT(per),allowed,max.). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{0.9\ tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)} \right)$$

For example, if the measured jitter into a LPDDR3-1600 device has tCK(avg) = 1250ps,tJIT(per),act,min = –92ps, and tJIT(per),act,max = +134ps, then

$$tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (134 - 100)/1250=0.8728\ tCK(avg)$$

tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal transition (DMn or DQm, where: n = 0, 1, 2, or 3; and m = DQ[31:0]), and specified timings must be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (for instance, tJIT(per)).

tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min. These parameters determine absolute Data-Valid Window (DVW) at the LPDDR3 device pin.

Absolute min DVW @ LPDDR3 device pin =

$$min\{ (tQSH(abs)min – tDQSQmax) , (tQSL(abs)min – tDQSQmax) \}$$

This minimum DVW shall be met at the target frequency regardless of clock jitter.

tRPST

tRPST is affected by duty cycle jitter, represented by tCL(abs). Therefore, tRPST(abs)min can be specified by tCL(abs)min.

$$tRPST(abs)min = tCL(abs)min - 0.05 = tQSL(abs)min$$

Clock Jitter Effects on WRITE Timing Parameters

tDS, tDH

These parameters are measured from a data signal (DMn or DQm, where n = 0, 1, 2, 3; and m = DQ[31:0]) transition edge to its respective data strobe signal (DQSn, $\overline{DQS}$n = 0,1,2,3) crossing. The specification values are not affected by the amount of tJIT(per) applied, as the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx, $\overline{DQS}$x) crossing to its respective clock signal (CK, $\overline{CK}$) crossing. The specification values are not affected by the amount of tJIT(per)) applied, as the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

tDQSS

This parameter is measured from a data strobe signal (DQSx, $\overline{DQS}$x) crossing to the subsequent clock signal (CK/$\overline{CK}$) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act,min - tJIT(per),allowed,min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example, if the measured jitter into an LPDDR3-1600 device has tCK(avg) = 1250ps,tJIT(per),act,min = -92ps, and tJIT(per),act,max = +134ps, then:

tDQSS,(min,derated) = 0.75 - (tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-93 + 100)/1250 = 0.7444 tCK(avg), and

tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (134 - 100)/1250 = 1.2228 tCK(avg).

REFRESH Requirements

LPDDR3 Refresh Requirement Parameters (Per density)

Parameter		Symbol	8 Gb	Unit
Number of Banks			8	-
Refresh Window: Tcase ≦ 85°C		**tREFW**	32	ms
Refresh Window: 85°C < Tcase ≦ 105°C		**tREFW**	8	ms
Required number of REFRESH commands (min)		**R**	8,192	-
Average time between REFRESH commands (for reference only) Tcase ≦ 85°C	REFab	**tREFI**	3.9	µs
	REFpb	**tREFIpb**	0.4875	µs
Average time between REFRESH commands (for reference only) 85°C < Tcase ≦ 105°C	REFab	**tREFI**	0.975	µs
	REFpb	**tREFIpb**	0.121875	µs
Refresh Cycle time		**tRFCab**	210	ns
Per Bank Refresh Cycle time		**tRFCpb**	90	ns

LPDDR3 Read and Write Latencies

Parameter	Value								Unit
Max. Clock Frequency	166	400	533	600	667	733	800	933	MHz
Max. Data Rate	333	800	1066	1200	1333	1466	1600	1866	Mbps
Average Clock Period	6	2.5	1.875	1.67	1.5	1.36	1.25	1.071	ns
Read Latency	3[1]	6	8	9	10	11	12	14	tCK(avg)
Write Latency (Set A)	1[1]	3	4	5	6	6	6	8	tCK(avg)
Write Latency (Set B)[2]	1[1]	3	4	5	8	9	9	11	tCK(avg)

NOTE 1 RL=3/WL=1 setting is an optional feature. Refer to MR0 OP<7>.

NOTE 2 Write Latency (Set B) support is an optional feature. Refer to MR0 OP<6>.

NOTE 3 Clock Frequency herewith is a reference base on JEDEC's. Precise setting needs to follow where defined on speed compatible table in section “Operating Frequency”, exceptional setting please confirm with NTC.

AC Timing

(Data rate 1866, 1600,1333 Specifications and conditions)

Notes 1–4 apply to all parameters. Notes begin below table.

Parameter	Symbol	Min/ Max	Data Rate			Unit
			1866	1600	1333	
Maximum clock frequency	***f*CK**	–	933	800	667	MHz
Clock Timing						
Average clock period	**tCK(avg)**	MIN	1.071	1.25	1.5	ns
		MAX	1.5	1.5	1.5	
Average HIGH pulse width	**tCH(avg)**	MIN	0.45			tCK(avg)
		MAX	0.55			
Average LOW pulse width	**tCL(avg)**	MIN	0.45			tCK(avg)
		MAX	0.55			
Absolute clock period	**tCK(abs)**	MIN	*tCK(avg) MIN + tJIT(per) MIN*			ns
Absolute clock HIGH pulse width	**tCH(abs)**	MIN	0.43			tCK(avg)
		MAX	0.57			
Absolute clock LOW pulse width	**tCL(abs)**	MIN	0.43			tCK(avg)
		MAX	0.57			
Clock period jitter (with supported jitter)	**tJIT(per)**, allowed	MIN	-60	-70	-80	ps
		MAX	60	70	80	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	**tJIT(cc)**, allowed	MAX	120	140	160	ps
Duty cycle jitter (with supported jitter)	**tJIT(duty)**, allowed	MIN	*min((tCH(abs),min -tCH(avg),min), (tCL(abs),min - tCL(avg),min)) × tCK(avg)*			ps
		MAX	*max((tCH(abs),max -tCH(avg),max), (tCL(abs),max - tCL(avg),max)) × tCK(avg)*			
Cumulative errors across 2 cycles	**tERR(2per)**, allowed	MIN	-88	-103	-118	ps
		MAX	88	103	118	
Cumulative errors across 3 cycles	**tERR(3per)**, allowed	MIN	-105	-122	-140	ps
		MAX	105	122	140	
Cumulative errors across 4 cycles	**tERR(4per)**, allowed	MIN	-117	-136	-155	ps
		MAX	117	136	155	
Cumulative errors across 5 cycles	**tERR(5per)**, allowed	MIN	-126	-147	-168	ps
		MAX	126	147	168	
Cumulative errors across 6 cycles	**tERR(6per)**, allowed	MIN	-133	-155	-177	ps
		MAX	133	155	177	
Cumulative errors across 7 cycles	**tERR(7per)**, allowed	MIN	-139	-163	-186	ps
		MAX	139	163	186	
Cumulative errors across 8 cycles	**tERR(8per)**, allowed	MIN	-145	-169	-193	ps
		MAX	145	169	193	
Cumulative errors across 9 cycles	**tERR(9per)**, allowed	MIN	-150	-175	-200	ps
		MAX	150	175	200	
Cumulative errors across 10 cycles	**tERR(10per)**, allowed	MIN	-154	-180	-205	ps
		MAX	154	180	205	
Cumulative errors across 11 cycles	**tERR(11per)**, allowed	MIN	-158	-184	-210	ps
		MAX	158	184	210	
Cumulative errors across 12 cycles	**tERR(12per)**, allowed	MIN	-161	-188	-215	ps
		MAX	161	188	215	

Parameter	Symbol	Min/ Max	Data Rate			Unit
			1866	1600	1333	
Clock Timing						
Cumulative errors across n = 13, 14, 15..., 19, 20 cycles	**tERR(nper)**, allowed	MIN	*tERR(nper),allowed MIN = (1 + 0.68ln(n)) ×tJIT(per), allowed MIN*			ps
		MAX	*tERR (nper), allowed MAX = (1 + 0.68ln(n)) ×tJIT(per), allowed MAX*			
ZQ Calibration Parameters						
Initialization calibration time	**tZQINIT**	MIN	1			µs
Long calibration time	**tZQCL**	MIN	360			ns
Short calibration time	**tZQCS**	MIN	90			ns
Calibration RESET time	**tZQRESET**	MIN	max(50ns,3*n*CK)			ns
READ Parameters[5]						
DQS output access time from CK/$\overline{CK}$	**tDQSCK**	MIN	2500			ps
		MAX	5500			
DQSCK delta short	**tDQSCKDS**	MAX	190	220	265	ps
DQSCK delta medium	**tDQSCKDM**	MAX	435	511	593	ps
DQSCK delta long	**tDQSCKDL**	MAX	525	614	733	ps
DQS-DQ skew	**tDQSQ**	MAX	115	135	165	ps
DQS output HIGH pulse width	**tQSH**	MIN	*tCH(abs)* - 0.05			tCK(avg)
DQS output LOW pulse width	**tQSL**	MIN	*tCL(abs)* - 0.05			tCK(avg)
DQ/DQS output hold time from DQS	**tQH**	MIN	min(*t*QSH, *t*QSL)			ps
READ preamble	**tRPRE**	MIN	0.9			tCK(avg)
READ postamble	**tRPST**	MIN	0.3			tCK(avg)
DQS Low-Z from clock	**tLZ(DQS)**	MIN	*t*DQSCK (MIN) - 300			ps
DQ Low-Z from clock	**tLZ(DQ)**	MIN	*t*DQSCK,(MIN) - 300			ps
DQS High-Z from clock	**tHZ(DQS)**	MAX	*t*DQSCK,(MAX) - 100			ps
DQ High-Z from clock	**tHZ(DQ)**	MAX	*t*DQSCK,(MAX) + (1.4 × *t*DQSQ,(MAX))			ps
WRITE Parameters[5]						
DQ and DM input hold time (VREF based)	**tDH**	MIN	130	150	175	ps
DQ and DM input setup time (VREF based)	**tDS**	MIN	130	150	175	ps
DQ and DM input pulse width	**tDIPW**	MIN	0.35			tCK(avg)
Write command to 1st DQS latching transition	**tDQSS**	MIN	0.75			tCK(avg)
		MAX	1.25			
DQS input high-level width	**tDQSH**	MIN	0.4			tCK(avg)
DQS input low-level width	**tDQSL**	MIN	0.4			tCK(avg)
DQS falling edge to CK setup time	**tDSS**	MIN	0.2			tCK(avg)
DQS falling edge hold time from CK	**tDSH**	MIN	0.2			tCK(avg)
Write postamble	**tWPST**	MIN	0.4			tCK(avg)
Write preamble	**tWPRE**	MIN	0.8			tCK(avg)
CKE Input Parameters						
CKE minimum pulse width (HIGH and LOW pulse width)	**tCKE**	MIN	max(7.5ns,3*n*CK)			ns
CKE input setup time	**tISCKE**	MIN	0.25			tCK(avg)
CKE input hold time	**tIHCKE**	MIN	0.25			tCK(avg)
Command path disable delay	**tCPDED**	MIN	2			tCK(avg)
Command Address Input Parameters[5]						
Address and control input setup time	**tISCA**	MIN	130	150	175	ps
Address and control input hold time	**tIHCA**	MIN	130	150	175	ps
$\overline{CS}$ input setup time	**tISCS**	MIN	230	270	290	ps
$\overline{CS}$ input hold time	**tIHCS**	MIN	230	270	290	ps

Parameter	Symbol	Min/ Max	Data Rate			Unit
			1866	1600	1333	
Command Address Input Parameters[5]						
Address and control input pulse width	**tIPWCA**	MIN	0.35			tCK(avg)
$\overline{CS}$ input pulse width	**tIPWCS**	MIN	0.7			tCK(avg)
Boot Parameters (10 MHz–55 MHz) [17, 18, 19]						
Clock cycle time	**tCK**b	MAX	100			ns
		MIN	18			
CKE input setup time	**tISCKE**b	MIN	2.5			ns
CKE input hold time	**tIHCKE**b	MIN	2.5			ns
Address and control input setup time	**tIS**b	MIN	1150			ps
Address and control input hold time	**tIH**b	MIN	1150			ps
DQS output data access time from CK/$\overline{CK}$	**tDQSCK**b	MIN	2			ns
		MAX	10			
Data strobe edge to output data edge	**tDQSQ**b	MAX	1.2			ns
Mode Register Parameters						
MODE REGISTER WRITE command period	**tMRW**	MIN	10			tCK(avg)
MODE REGISTER READ command period	**tMRR**	MIN	4			tCK(avg)
Additional time after tXP has expired until the MRR command may be issued	**tMRRI**	MIN	*t*RCD(min)			ns
Core Parameters [20]						
READ latency	**RL**	MIN	14	12	10	tCK(avg)
WRITE latency(Set A)	**WL**	MIN	8	6	6	tCK(avg)
WRITE latency(Set B)	**WL**	MIN	11	9	8	tCK(avg)
ACTIVATE-to- ACTIVATE command period	**tRC**	MIN	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)			ns
CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	**tCKESR**	MIN	max(15ns,3*n*CK)			ns
SELF REFRESH exit to next valid command delay	**tXSR**	MIN	max(*t*RFCab + 10ns,2*n*CK)			ns
Exit power- down to next valid command delay	**tXP**	MIN	max(7.5ns,3*n*CK)			ns
CAS-to-CAS delay	**tCCD**	MIN	4			tCK(avg)
Internal READ to PRECHARGE command delay	**tRTP**	MIN	max(7.5ns,4*n*CK)			ns
RAS-to-CAS delay	**tRCD** (typ)	MIN	max(18ns,3*n*CK)			ns
Row precharge time (single bank)	**tRP**pb (typ)	MIN	max(18ns,3*n*CK)			ns
Row precharge time (all banks)	**tRP**pab (typ)	MIN	max(21ns,3*n*CK)			ns
Row active time	**tRAS**	MIN	max(42ns,3*n*CK)			ns
		MAX	70			µs
WRITE recovery time	**tWR**	MIN	max(15ns,4*n*CK)			ns
Internal WRITE-to- READ command delay	**tWTR**	MIN	max(7.5ns,4*n*CK)			ns
Active bank A to active bank B	**tRRD**	MIN	max(10ns,2*n*CK)			ns
Four-bank ACTIVATE window	**tFAW**	MIN	max(50ns,8*n*CK)			ns
Minimum deep power- down time	**tDPD**	MIN	500			µs

Parameter	Symbol	Min/ Max	Data Rate			Unit
			1866	1600	1333	
ODT Parameters						
Asynchronous R_{TT} turn-on dely from ODT input	**tODT**on	MIN	1.75			ns
		MAX	3.5			
Asynchronous R_{TT} turn-off delay from ODT input	**tODT**off	MIN	1.75			ns
		MAX	3.5			
Automatic R_{TT} turn-on delay after READ data	**tAODT**on	MAX	*t*DQSCK + 1.4 × *t*DQSQ,max + *t*CK(avg,min)			ps
Automatic R_{TT} turn-off delay after READ data	**tAODT**off	MIN	*t*DQSCK,min - 300			ps
R_{TT} disable delay from power down, self-refresh, and deep power down entry	**tODT**d	MIN	12			ns
R_{TT} enable delay from power down and self refresh exit	**tODT**e	MAX	12			ns
CA Training Parameters						
First CA calibration command after CA calibration mode is programmed	**tCAMRD**	MIN	20			tCK(avg)
First CA calibration command after CKE is LOW	**tCAENT**	MIN	10			tCK(avg)
CA caibration exit command after CKE is HIGH	**tCAEXT**	MIN	10			tCK(avg)
CKE LOW after CA calibration mode is programmed	**tCACKEL**	MIN	10			tCK(avg)
CKE HIGH after the last CA calibration results are driven.	**tCACKEH**	MIN	10			tCK(avg)
Data out delay after CA training calibration command is programmed	**tADR**	MAX	20			ns
MRW CA exit command to DQ tri-state	**tMRZ**	MIN	3			ns
CA calibration command to CA calibration command delay	**tCACD**	MIN	RU(*t*ADR+2 × *t*CK)			tCK(avg)
Write Leveling Parameters						
DQS/$\overline{\text{DQS}}$ delay after write leveling mode is programmed	**tWLDQSEN**	MIN	25			ns
		MAX	—			
First DQS/$\overline{\text{DQS}}$ edge after write leveling mode is programmed	**tWLMRD**	MIN	40			ns
		MAX	—			
Write leveling output delay	**tWLO**	MIN	0			ns
		MAX	20			
Write leveling hold time	**tWLH**	MIN	150	175	205	ps
Write leveling setup time	**tWLS**	MIN	150	175	205	ps
Mode register set command delay	**tMRD**	MIN	MAX (14ns, 10nCK)			ns
		MAX	—			
Temperature Derating						
DQS output access time from CK/$\overline{\text{CK}}$ (derated)	**tDQSCK**	MAX	5620			ps
RAS-to-CAS delay (derated)	**tRCD**	MIN	*t*RCD + 1.875			ns
ACTIVATE-to-ACTIVATE command period (derated)	**tRC**	MIN	*t*RC + 1.875			ns
Row active time (derated)	**tRAS**	MIN	*t*RAS + 1.875			ns
Row precharge time (derated)	**tRP**	MIN	*t*RP + 1.875			ns
Active bank A to active bank B (derated)	**tRRD**	MIN	*t*RRD + 1.875			ns

NOTE 1 Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.

NOTE 2 All AC timings assume an input slew rate of 2V/ns for single-ended signals.

NOTE 3 Measured with 4 V/ns differential CK/$\overline{\text{CK}}$ slew rate and nominal VIX.

NOTE 4 All timing and voltage measurements are defined at the ball.

NOTE 5 READ, WRITE, and input setup and hold values are referenced to VREF.

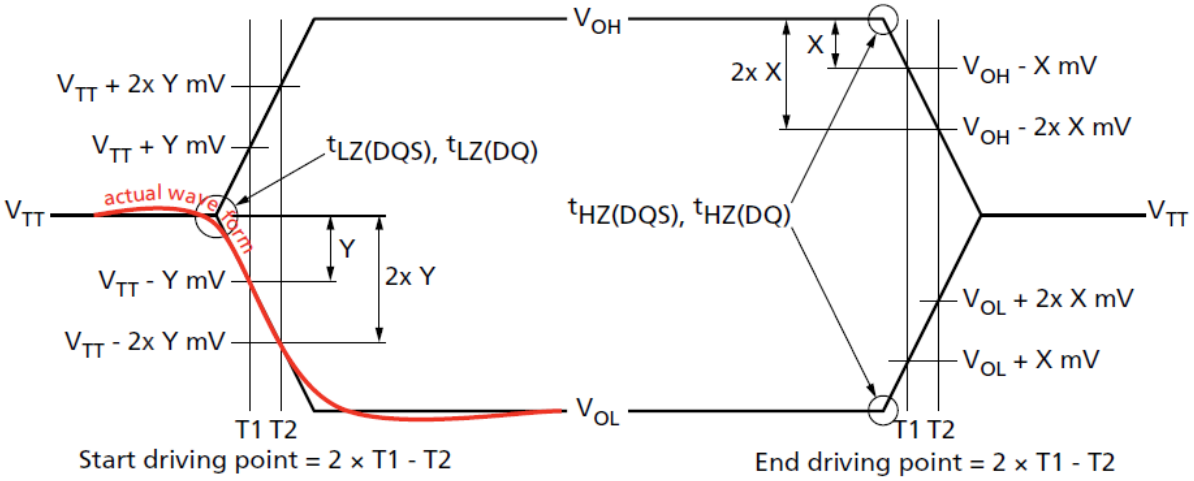
NOTE 6 tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is <10°C/s. Values do not include clock jitter.

NOTE 7 tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is <10°C/s. Values do not include clock jitter.

NOTE 8 tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is <10°C/s. Values do not include clock jitter.

NOTE 9 For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS) and tLZ(DQ)). The figure below shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ) or begins driving tLZ(DQS) and tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

NOTE 10 Output Transition Timing



NOTE 11 The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS/$\overline{\text{DQS}}$.

NOTE 12 Measured from the point when DQS/$\overline{\text{DQS}}$ begins driving the signal, to the point when DQS/$\overline{\text{DQS}}$ begins driving the first rising strobe edge.

NOTE 13 Measured from the last falling strobe edge of DQS/$\overline{\text{DQS}}$ to the point when DQS/$\overline{\text{DQS}}$ finishes driving the signal.

NOTE 14 CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK/$\overline{\text{CK}}$ crossing.

NOTE 15 CKE input hold time is measured from CK/$\overline{\text{CK}}$ crossing to CKE reaching a HIGH/LOW voltage level.

NOTE 16 Input setup/hold time for signal (CA[9:0], $\overline{\text{CS}}$).

NOTE 17 To ensure device operation before the device is configured, a number of AC boot timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).

NOTE 18 Mobile LPDDR3 devices set some mode register default values upon receiving a RESET (MRW) command, as specified in Mode Register Definition.

NOTE 19 The output skew parameters are measured with default output impedance settings using the reference load.

NOTE 20 The minimum tCK column applies only when tCK is greater than 6ns.

CA and $\overline{CS}$ Setup, Hold and Derating

For all input signals (CA and $\overline{CS}$) the total t_{IS} (setup time) and t_{IH} (hold time) required is calculated by adding the data sheet t_{IS}(base) and t_{IH}(base) value (see tIS/tIH Base Table) to the Δt_{IS} and Δt_{IH} derating value (see tIS/tIH Derating Table) respectively. Example: t_{IS} (total setup time) = t_{IS}(base) + Δt_{IS}.

Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see following typical slew rate Figure of tIS). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see following angent line figure of tIS).

Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see following typical slew rate Figure of tIH). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see following angent line figure of tIH).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see table of required tVAC for CA).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$. For slew rates in between the values listed in derating Table, the derating values may be obtained by linear interpolation. These values are typically not subject to production test. They are verified.

CA Setup and Hold Base-Values

unit [ps]	Data Rate			reference
	1866	1600	1333	
*t*ISCA(base)	-	75	100	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-150mV
*t*ISCA(base)	62.5	-	-	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-135mV
*t*IHCA(base)	80	100	125	$V_{IH/L(dc)} = V_{REF(dc)}$ +/-100mV

NOTE 1 AC/DC referenced for 2V/ns CA slew rate and 4V/ns differential CK-$\overline{CK}$ slew rate.

$\overline{CS}$ Setup and Hold Base-Values

unit [ps]	Data Rate			reference
	1866	1600	1333	
*t*ISCS(base)	-	195	215	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-150mV
*t*ISCS(base)	162.5	-	-	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-135mV
*t*IHCS(base)	180	220	240	$V_{IH/L(dc)} = V_{REF(dc)}$ +/-100mV

NOTE 1 AC/DC referenced for 2V/ns $\overline{CS}$ slew rate and 4V/ns differential CK-$\overline{CK}$ slew rate.

Derating values tIS/tIH - ac/dc based AC150

ΔtISCA, ΔtIHCA, ΔtISCS, ΔtIHCS derating in [ps] AC/DC based AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV													
		CK, $\overline{CK}$ Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA,$\overline{CS}$ Slew rate (V/ns)	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	3.0	-	-	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1 Cell contents shaded in pink are defined as ‘not supported’.

Derating values tIS/tIH - ac/dc based AC135

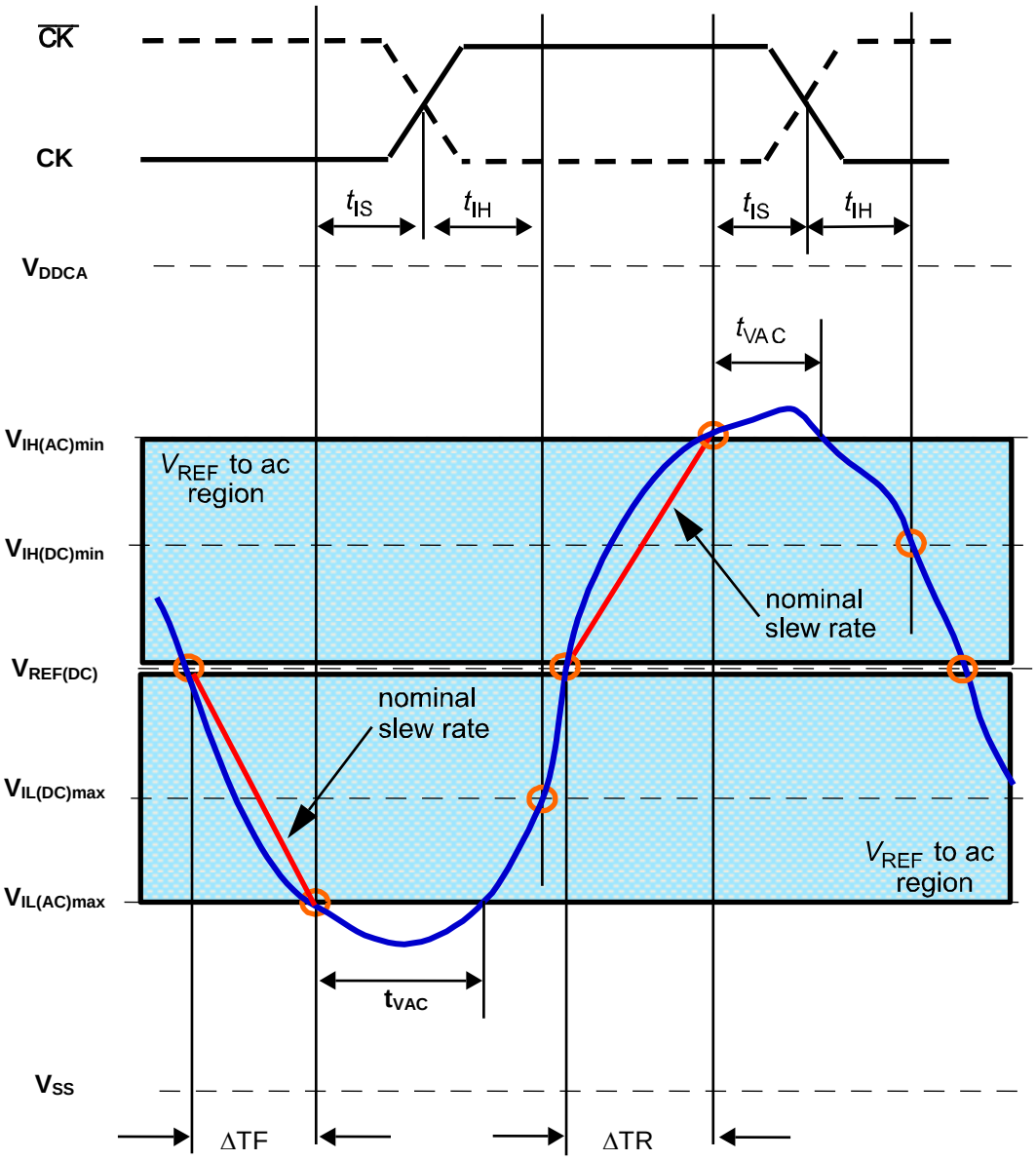
ΔtISCA, ΔtIHCA, ΔtISCS, ΔtIHCS derating in [ps] AC/DC based AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV													
		CK, $\overline{CK}$ Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA,$\overline{CS}$ Slew rate (V/ns)	4.0	34	25	34	25	34	25	34	25	34	25	-	-
	3.0	-	-	23	17	23	17	23	17	23	17	34	29
	2.0	-	-	-	-	0	0	0	0	0	0	11	13
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	-12	-4

NOTE 1 Cell contents shaded in pink are defined as ‘not supported’.

Required time *t*VAC above *V*IH(ac) {below *V*IL(ac)} for valid transition for CA

Slew Rate (V/ns)	tVAC at 135mV (ps) 1866Mb/s		tVAC at 150mV (ps) 1600Mb/s		tVAC at 150mV (ps) 1333Mb/s	
	Min	Max	Min	Max	Min	Max
>4.0	40	—	48	—	58	—
4.0	40	—	48	—	58	—
3.5	39	—	46	—	56	—
3.0	36	—	43	—	53	—
2.5	33	—	40	—	50	—
2.0	29	—	35	—	45	—
1.5	21	—	27	—	37	—
<1.5	21	—	27	—	37	—

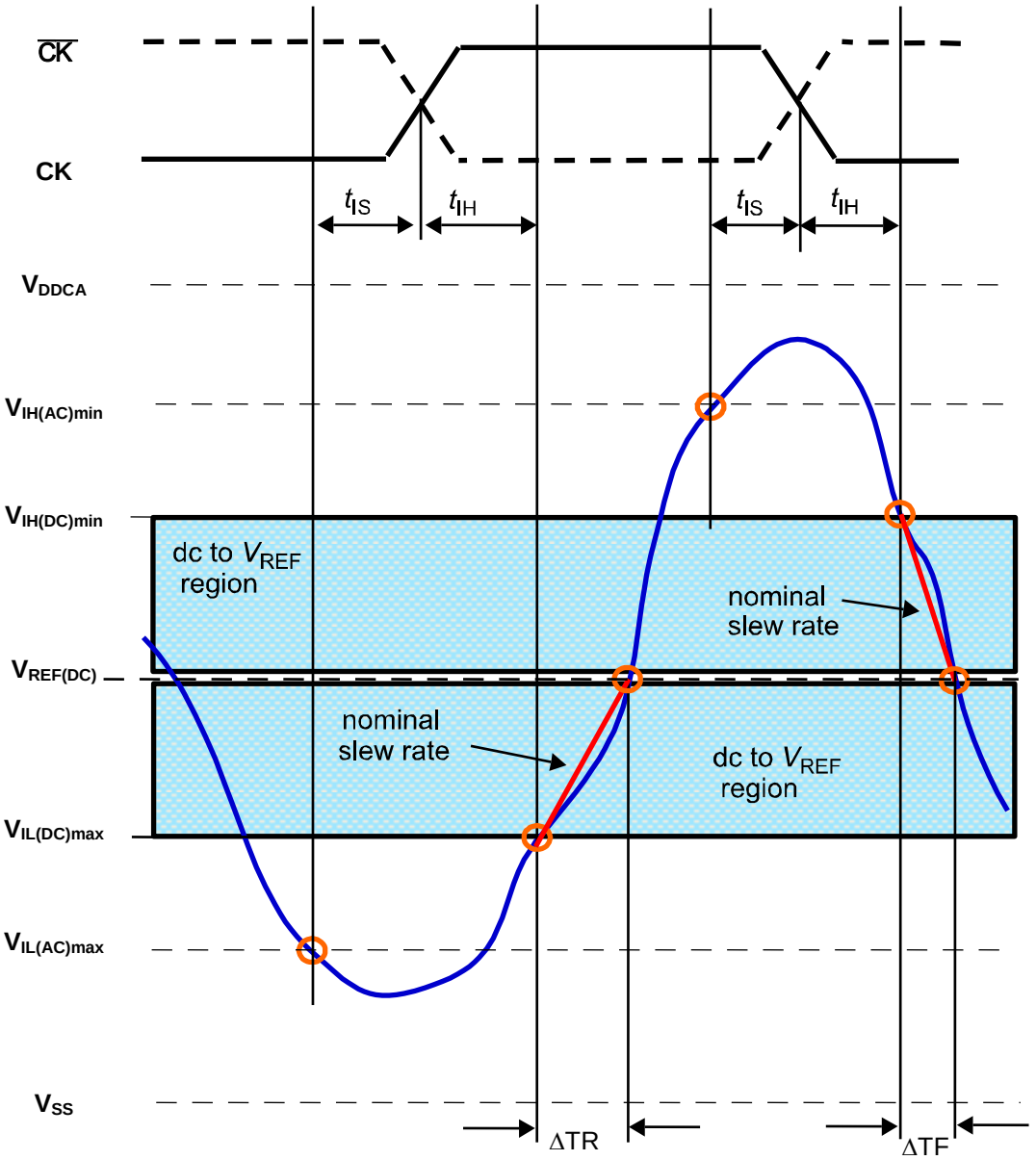
Typical Slew Rate and tVAC – tIS for CA and $\overline{CS}$ Relative to Clock



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}\text{max}}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}\text{min} - V_{REF(dc)}}{\Delta TR}$$

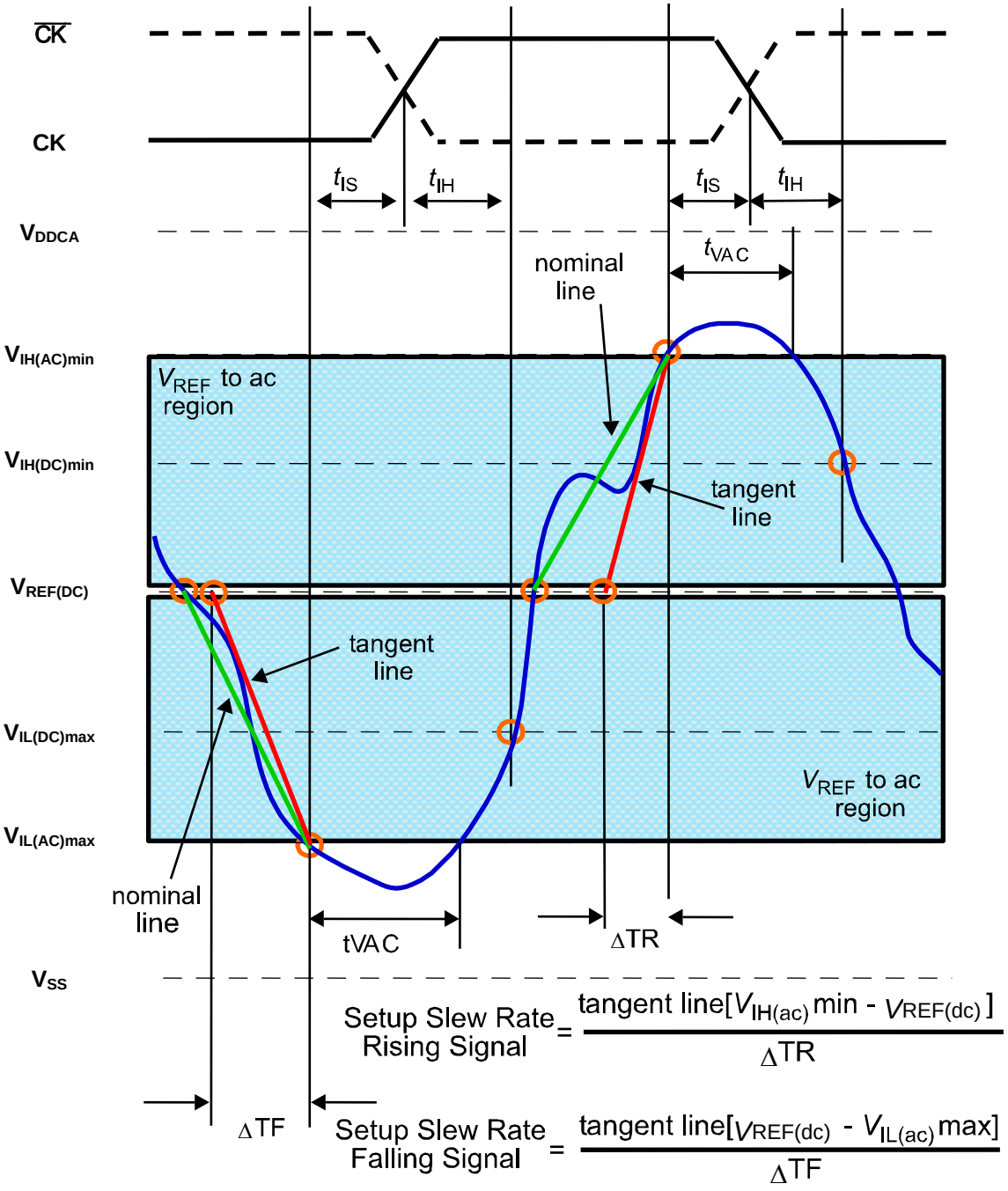
Typical Slew Rate – tIH for CA and $\overline{CS}$ Relative to Clock



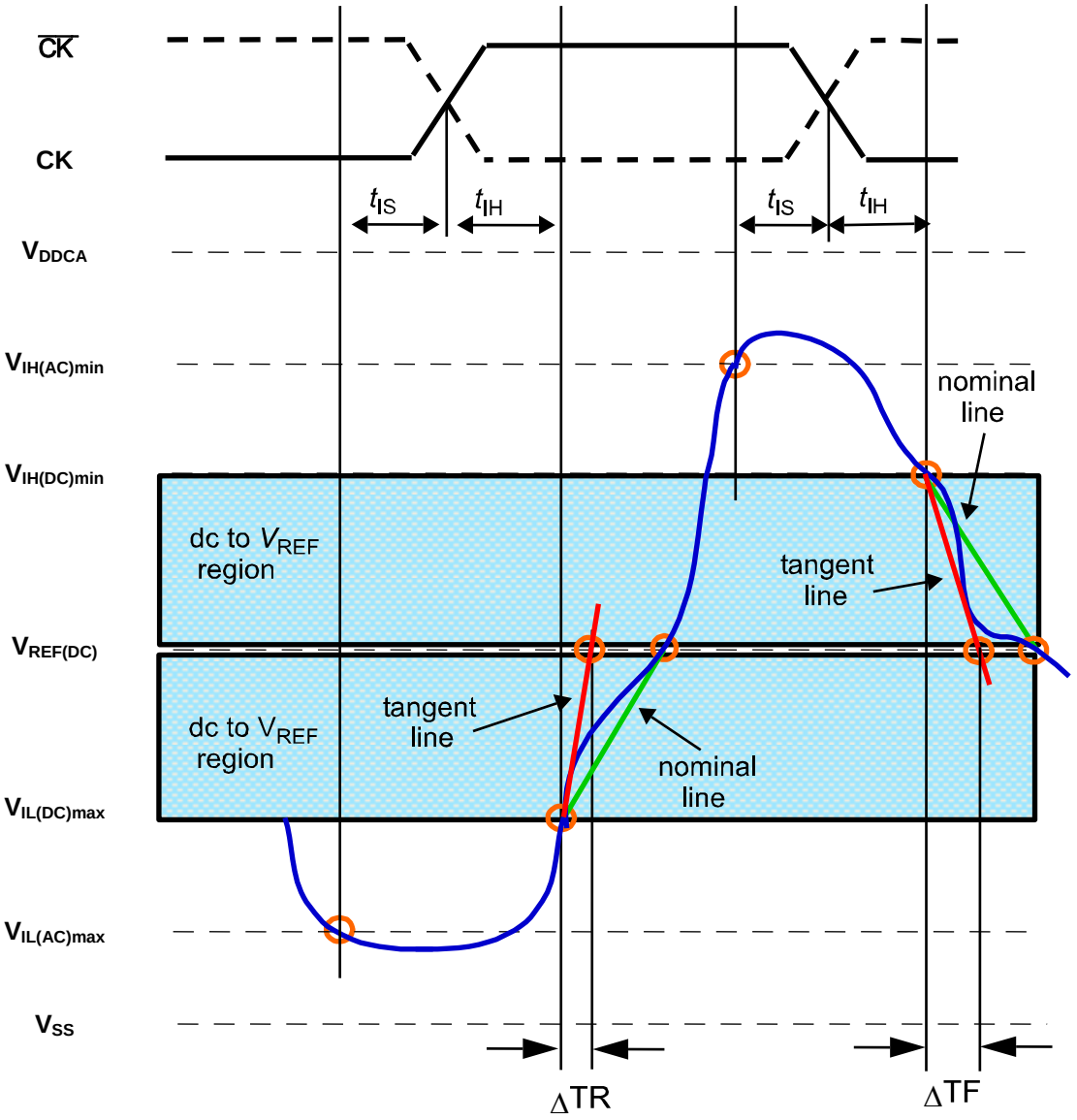
$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}\text{max}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}\text{min} - V_{REF(dc)}}{\Delta TF}$$

Tangent Line – tIS for CA and $\overline{CS}$ Relative to Clock



Tangent Line – tIH for CA and $\overline{CS}$ Relative to Clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{REF(dc)} - V_{IL(dc)}\text{max]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [} V_{IH(dc)}\text{min - } V_{REF(dc)}\text{]}}{\Delta TF}$$

Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total t_{DS} (setup time) and t_{DH} (hold time) required is calculated by adding the data sheet t_{DS}(base) and t_{DH}(base) value (see the following tDS/tDH base table) to the Δt_{DS} and Δt_{DH} (see tDS/tDH derating table) derating value respectively. Example: t_{DS} (total setup time) = t_{DS}(base) + Δt_{DS}.

Setup (t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see following typical slew rate Figure of tDS). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value(see following angent line figure of tDS).

Hold (t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}$max and the first crossing of $V_{REF(dc)}$. Hold (t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)}$min and the first crossing of $V_{REF(dc)}$ (see following typical slew rate Figure of tDH). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see following angent line figure of tDH).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see table of required tVAC for DQ/DM).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the tables the derating values may be obtained by linear interpolation.

These values are typically not subject to production test. They are verified.

Data Setup and Hold Base-Values (>400MHz, 1V/ns Slew Rate)

unit [ps]	Data Rate			reference
	1866	1600	1333	
tDS(base)	-	75	100	$V_{IH/L(ac)}$ = $V_{REF(dc)}$ +/- 150mV
tDS(base)	62.5	-	-	$V_{IH/L(ac)}$ = $V_{REF(dc)}$ +/- 135mV
tDH(base)	80	100	125	$V_{IH/L(dc)}$ = $V_{REF(dc)}$ +/- 100mV

NOTE 1 AC/DC referenced for 2V/ns DQ, DM slew rate and 4V/ns differential DQS-$\overline{DQS}$ slew rate and nominal V_{IX}.

Derating values tDS/tDH - ac/dc based AC150

ΔtDS, ΔtDH derating in [ps] AC/DC based AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV													
		DQS, $\overline{DQS}$ Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew rate (V/ns)	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	3.0	-	-	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1 Cell contents shaded in pink are defined as 'not supported'.

Derating values tDS/tDH - ac/dc based AC135

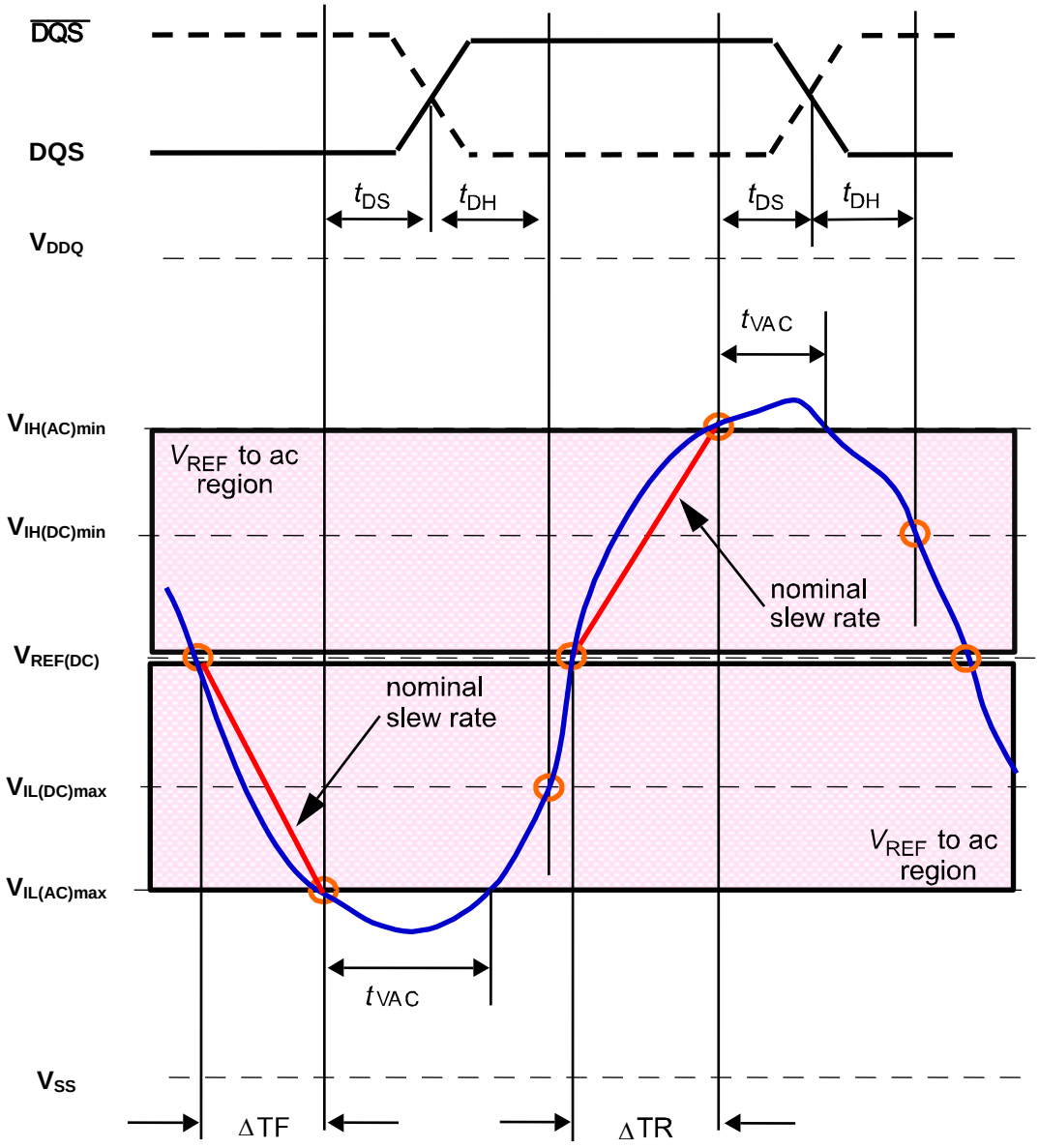
ΔtDS, ΔtDH derating in [ps] AC/DC based AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV													
		DQS, $\overline{DQS}$ Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew rate (V/ns)	4.0	34	25	34	25	34	25	34	25	34	25	-	-
	3.0	-	-	23	17	23	17	23	17	23	17	34	29
	2.0	-	-	-	-	0	0	0	0	0	0	11	13
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	-12	-4

NOTE 1 Cell contents shaded in pink are defined as 'not supported'.

Required time *t*VAC above *V*IH(ac) {below *V*IL(ac)} for valid transition for DQ, DM

Slew Rate (V/ns)	tVAC at 135mV (ps) 1866Mb/s		tVAC at 150mV (ps) 1600Mb/s		tVAC at 150mV (ps) 1333Mb/s	
	Min	Max	Min	Max	Min	Max
>4.0	40	—	48	—	58	—
4.0	40	—	48	—	58	—
3.5	39	—	46	—	56	—
3.0	36	—	43	—	53	—
2.5	33	—	40	—	50	—
2.0	29	—	35	—	45	—
1.5	21	—	27	—	37	—
<1.5	21	—	27	—	37	—

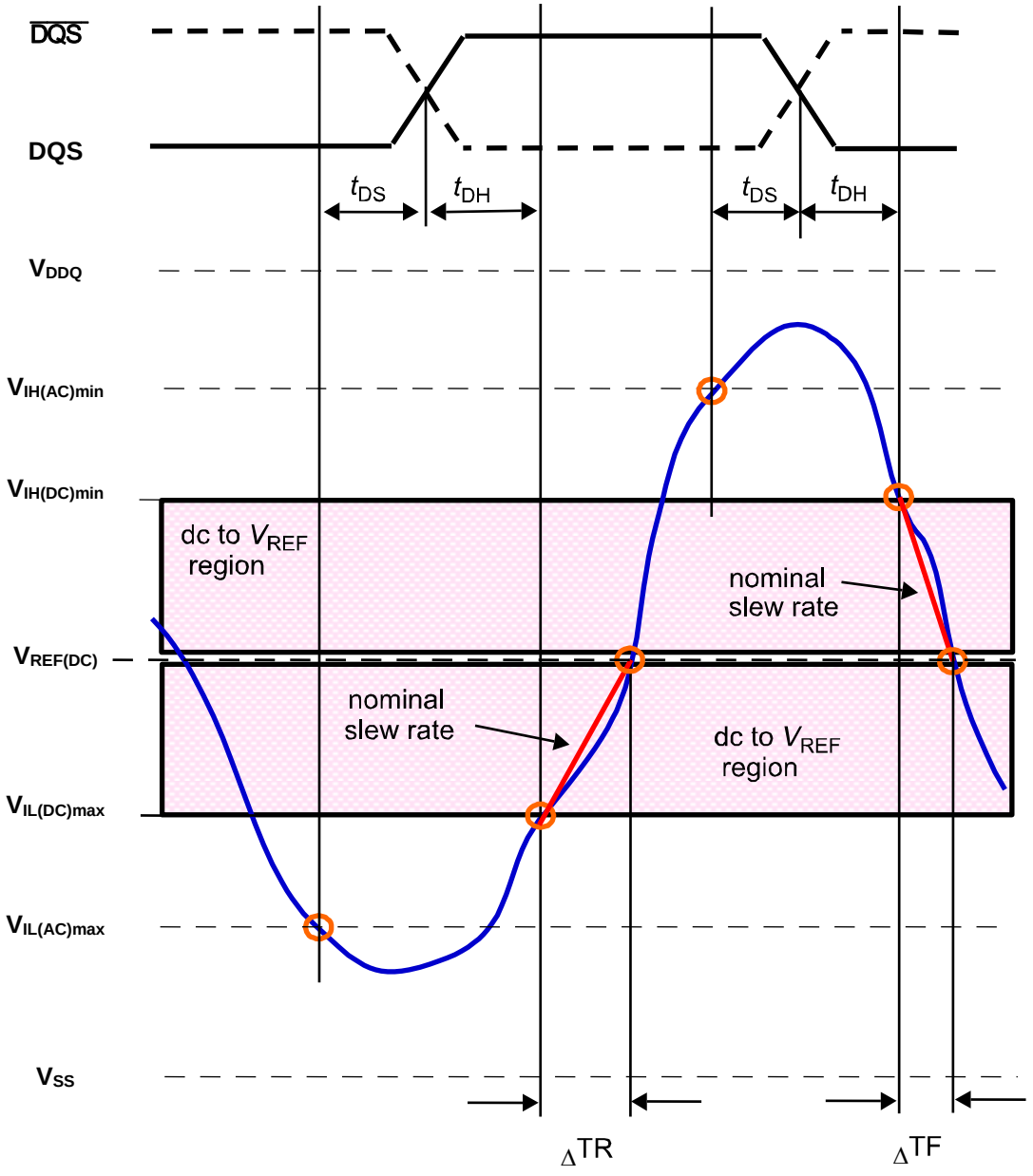
Typical Slew Rate and tVAC – tDS for DQ Relative to Strobe



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}\text{max}}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}\text{min} - V_{REF(dc)}}{\Delta TR}$$

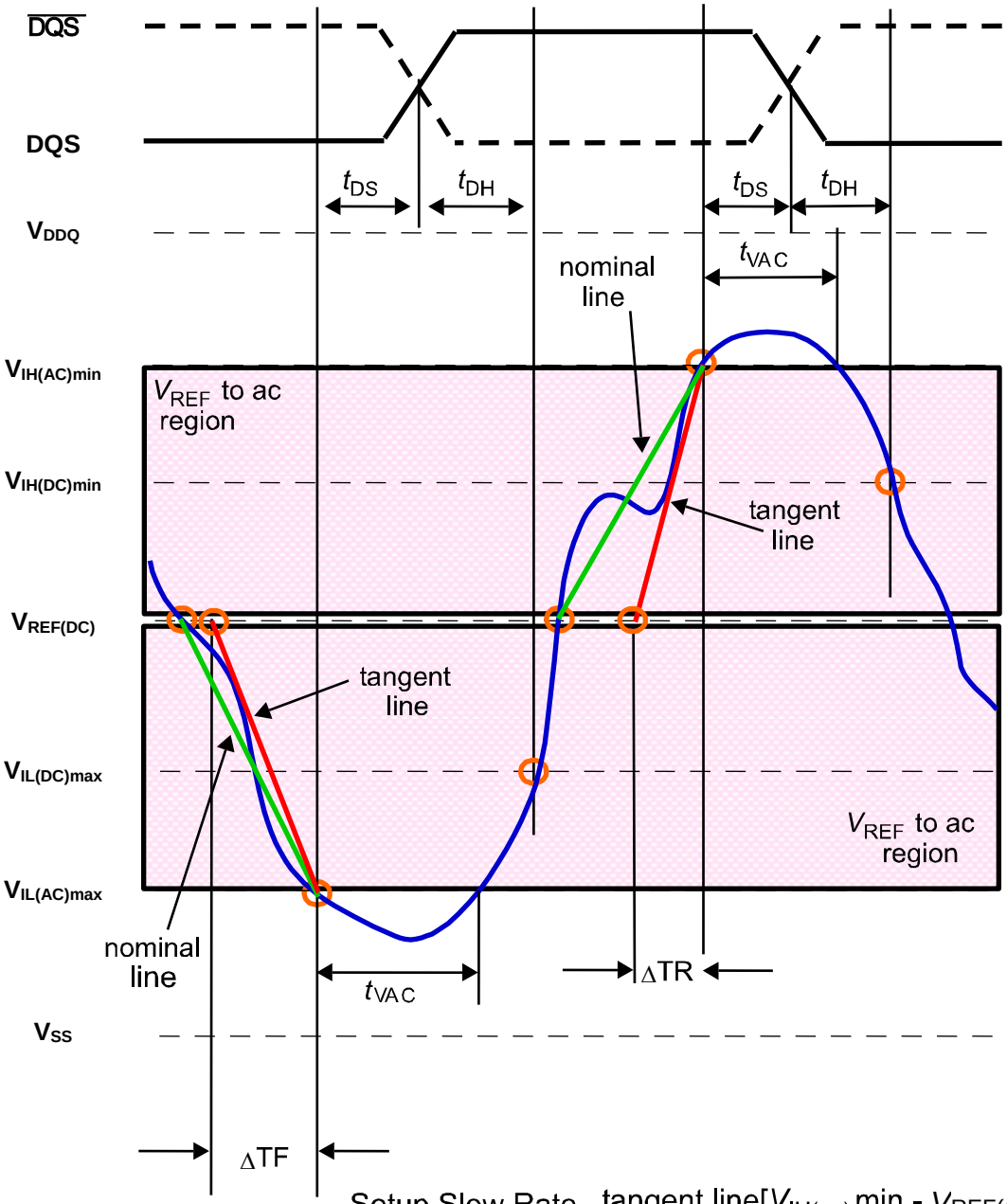
Typical Slew Rate – tDH for DQ Relative to Strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}\text{max}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}\text{min} - V_{REF(dc)}}{\Delta TF}$$

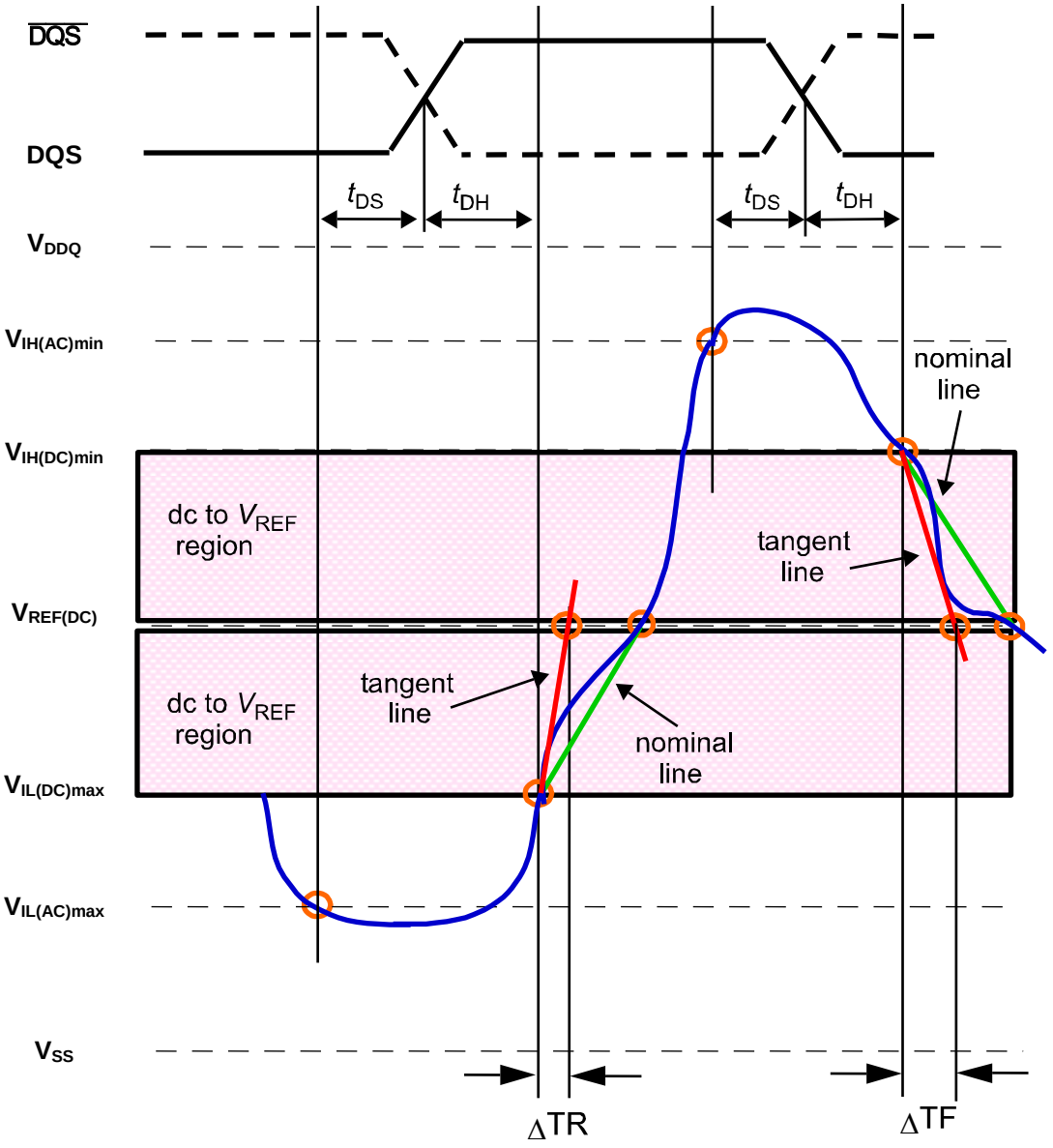
Tangent Line – tDS for DQ with Respect to Strobe



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line}[V_{IH(ac)}\text{min} - V_{REF(dc)}]}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line}[V_{REF(dc)} - V_{IL(ac)}\text{max}]}{\Delta TF}$$

Tangent Line – tDH for DQ with Respect for Strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [\, V_{REF(dc)} - V_{IL(dc)}\text{max} \,]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [\, V_{IH(dc)}\text{min} - V_{REF(dc)} \,]}{\Delta TF}$$

Basic Functionality

Mobile LPDDR3 is a high-speed SDRAM internally configured as an 8-bank memory device.

LPDDR3 uses a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

LPDDR3 uses a double data rate architecture on the DQ pins to achieve high-speed operation. The double data rate architecture is essentially an 8n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins.

A single read or write access for LPDDR3 effectively consists of a single 8n-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and eight corresponding nbit- wide, one-half-clock-cycle data transfers at the I/O pins. Read and write accesses to the device are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command followed by a READ or WRITE command. The address and BA bits registered coincident with the ACTIVATE command are used to select the row and bank to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Power-Up, Initialization, and Power-Off

LPDDR3 devices must be powered up and initialized in a predefined manner. Power-up and initialization by means other than those specified will result in undefined operation.

Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory and applies to devices.

1) Voltage Ramp:

While applying power (after Ta), CKE must be held LOW (≤ 0.2 × VDDCA), and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. Following the completion of the voltage ramp (Tb), CKE must be maintained LOW. DQ, DM, DQS and $\overline{\text{DQS}}$ voltage levels must be between VSS and VDDQ during voltage ramp to avoid latch up. CK, $\overline{\text{CK}}$, $\overline{\text{CS}}$, and CA input levels must be between VSS and VDDCA during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided below.

Voltage Ramp Conditions

After…	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2} (200 mV)
	V_{DD1} and V_{DD2} must be greater than V_{DDCA} (200 mV)
	V_{DD1} and V_{DD2} must be greater than V_{DDQ} (200 mV)
	V_{REF} must always be less than all other supply voltages
Notes: 1. Ta is the point when any power supply first reaches 300 mV. 2. Noted conditions apply between Ta and power-down (controlled or uncontrolled). 3. Tb is the point at which all supply and reference voltages are within their defined operating ranges. 4. Power ramp duration tINIT0 (Tb – Ta) must not exceed 20ms. 5. The voltage difference between any of VSS pins must not exceed 100 mV.	

Beginning at Tb, CKE must remain LOW for at least tINIT1, after which CKE can be asserted HIGH. The clock must be stable at least tINIT2 prior to the first CKE LOW-to-HIGH transition (Tc). CKE, $\overline{\text{CS}}$, and CA inputs must observe setup and hold requirements (tIS, tIH) with respect to the first rising clock edge (as well as to subsequent falling and rising edges).

If any MRRs are issued, the clock period must be within the range defined for tCKb. MRW commands can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least tINIT3 (Td). The ODT input signal may be in undefined state until *t*IS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal shall be statically held at either LOW or HIGH. The ODT input signal remains static until the power up initialization sequence is finished, including the expiration of *t*ZQINIT.

2) RESET Command:

After tINIT3 is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least tINIT4 while keeping CKE asserted and issuing NOP commands.

3) MRRs and Device Auto Initialization (DAI) Polling:

After tINIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications. Use the MRR command to poll the DAI bit and report when device auto initialization is complete; otherwise, the controller must wait a minimum of tINIT5, or until the DAI bit is set before proceeding. As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured. After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than tINIT5 after the RESET command. The controller must wait at least tINIT5 or until the DAI bit is set before proceeding.

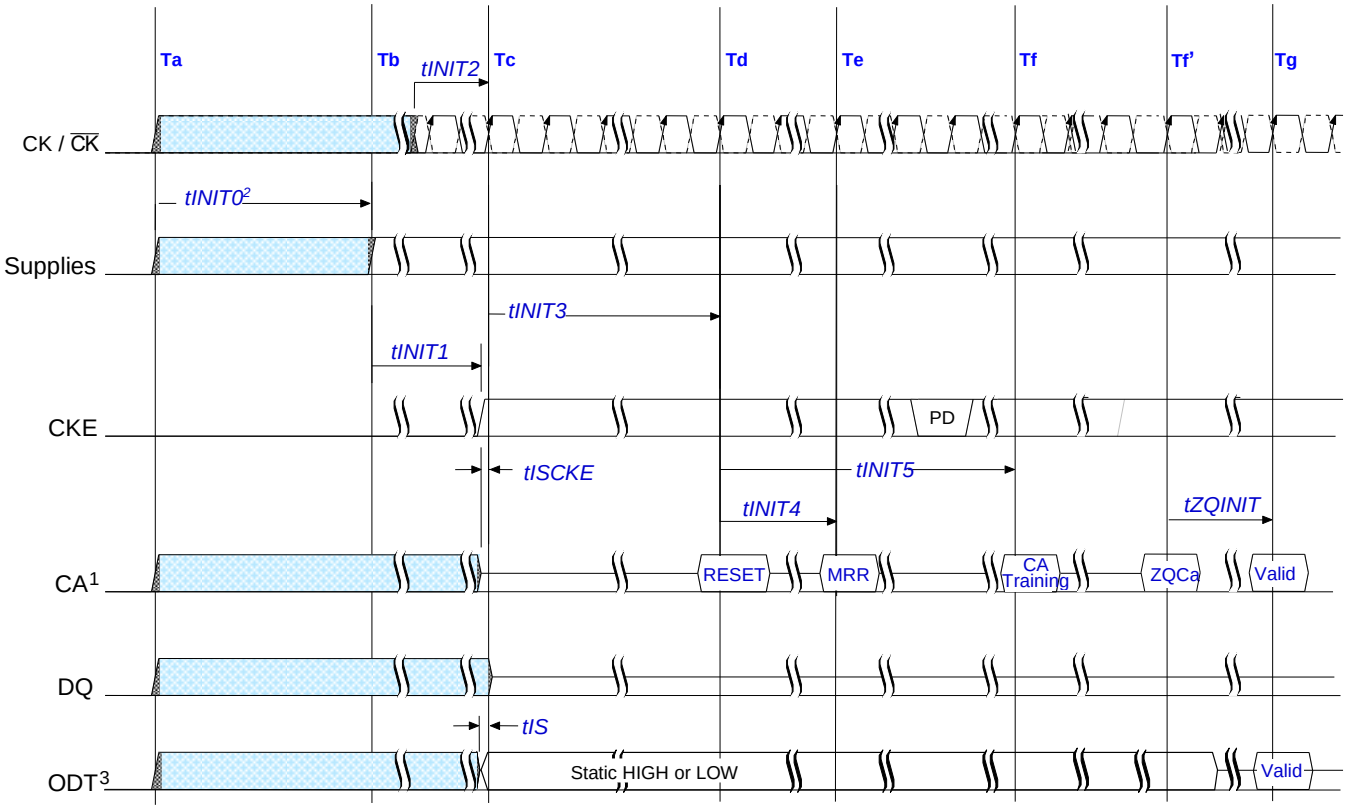
4) ZQ Calibration:

After tINIT5 (Tf), the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10). This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR3 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after tZQinit.

5) Normal Operation:

After tZQinit (Tg), MRW commands must be used to properly configure the memory (for example the output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in the LPDDR3 specification.

Power Ramp and Initialization Sequence



* Midlevel on CA bus means: valid NOP

NOTE 1 High-Z on the CA bus indicates NOP.

NOTE 2 For tINIT values, see below table.

NOTE 3 After RESET command (time Te), *R*TT is disabled until ODT function is enabled by MRW to MR11 following Tg.

NOTE 4 CA Training is optional.

Initialization Timing Parameters

Symbol	Parameter	Value		Unit
		min	max	
^{t}INIT0	Maximum Power Ramp Time	-	20	ms
^{t}INIT1	Minimum CKE low time after completion of power ramp	100	-	ns
^{t}INIT2	Minimum stable clock before first CKE high	5	-	tCK
^{t}INIT3	Minimum idle time after first CKE assertion	200	-	us
^{t}INIT4	Minimum idle time after Reset command	1	-	us
^{t}INIT5[1]	Maximum duration of Device Auto-Initialization	-	10	us
^{t}ZQINIT	ZQ Initial Calibration	1	-	us
^{t}CKb	Clock cycle time during boot	18	100	ns

NOTE 1 If DAI bit is not read via MRR, SDRAM will be in idle state after tINIT5(max) has expired.

Initialization after RESET (without voltage ramp):

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

Power-Off Sequence

The following procedure is required to power off the device. While powering off, CKE must be held LOW (≤ 0.2 × VDDCA); all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS, and $\overline{DQS}$ voltage levels must be between VSS and VDDQ during the power-off sequence to avoid latch-up. CK, $\overline{CK}$, $\overline{CS}$, and CA input levels must be between VSS and VDDCA during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

Power Supply Conditions

Between…	Applicable Conditions
Tx and Tz	VDD1 must be greater than VDD2—200 mV
Tx and Tz	VDD1 must be greater than VDDCA—200 mV
Tx and Tz	VDD1 must be greater than VDDQ—200 mV
Tx and Tz	VREF must always be less than all other supply voltages

Notes:

1. The voltage difference between any of VSS pins must not exceed 100 mV.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300 mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/µs between Tx and Tz. An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Power-Off Timing

Symbol	Parameter	Min	Max	Unit
t_{POFF}	Maximum power-off ramp time	-	2	s

Mode Register Definition

LPDDR3 devices contain a set of mode registers used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignment and Definition

Table below shows the mode registers. Each register is denoted as “R”, if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. Mode Register Read Command shall be used to read a register. Mode Register Write Command shall be used to write a register.

Mode Register Assignment

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info	R	RL3	WL-B	(RFU)	RZQI		(RFU)		DAI
1	01_H	Device Feature1	W	nWR (for AP)			(RFU)		BL		
2	02_H	Device Feature2	W	WRLev	WL Sel	(RFU)	nWRE		RL & WL		
3	03_H	I/O Config-1	W	(RFU)					DS		
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05_H	Basic Config-1	R	Manufacturer ID							
6	06_H	Basic Config-2	R	Revision ID1							
7	07_H	Basic Config-3	R	Revision ID2							
8	08_H	Basic Config-4	R	I/O width		Density				Type	
9	09_H	Test Mode	W	Vendor-Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11	$0B_H$	ODT	W	(RFU)					PD ctl	DQ ODT	
12-15	$0C_H$-$0F_H$	(Reserved)	—	(RFU)							
16	10_H	PASR_BANK	W	PASR Bank Mask							
17	11_H	PASR_Seg	W	PASR Segment Mask							
18-31	12_H-$1F_H$	(Reserved)	—	(RFU)							
32	20_H	DQ calibration pattern A	R	See Data Calibration Pattern Description							
33-39	21_H-27_H	(Do Not Use)	—	(DNU)							
40	28_H	DQ calibration pattern B	R	See Data Calibration Pattern Description							
41	29_H	CA Training 1	W	See MRW – CA Training Mode							
42	$2A_H$	CA Training 2	W	See MRW – CA Training Mode							
43-47	$2B_H$-$2F_H$	(Do Not Use)	—	(DNU)							
48	30_H	CA Training 3	W	See MRW – CA Training Mode							
49-62	31_H-$3E_H$	(Reserved)	—	(RFU)							
63	$3F_H$	RESET	W	X or 0xFCh							
64-255	40_H-FF_H	(Reserved)	—	(RFU)							

NOTE 1 RFU bits shall be set to '0' during mode register writes.

NOTE 2 RFU bits shall be read as '0' during mode register reads.

NOTE 3 All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS, $\overline{DQS}$ shall be toggled.

NOTE 4 All mode registers that are specified as RFU shall not be written.

NOTE 5 See vendor device datasheets for details on vendor-specific mode registers.

NOTE 6 Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA[7:0] = 00_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info	R	RL3	WL-B	(RFU)	RZQI		(RFU)		DAI

Feature	Register Information	Type	OP	Definition
DAI	Device Auto-Initialization Status	Read-only	OP<0>	0_B: DAI complete 1_B: DAI still in progress
RZQI[1-4]	RZQI (Built in Self Test for RZQ Information)	Read-only	OP<4:3>	00_B: RZQ self test not supported 01_B: ZQ-pin may connect to V_{DDCA} or float 10_B: ZQ-pin may short to GND 11_B: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to V_{DDCA} or float nor short to GND)
WL-B	WL (Set B) Support	Read-only	OP<6>	0B: DRAM does not support WL (Set B) 1B: DRAM supports WL (SetB)
RL3	RL3 Option Support	Read-only	OP<7>	0_B: DRAM does not support RL=3, nWR=3, WL=1 1_B: DRAM supports RL=3, nWR=3, WL=1 for frequencies ≤ 166

NOTE 1 RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.

NOTE 2 If ZQ is connected to V_{DDCA} to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to V_{DDCA}, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

NOTE 3 In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR3 device will default to factory trim settings for R_{ON}, and will ignore ZQ calibration commands. In either case, the system may not function as intended.

NOTE 4 In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240-Ω ±1%).

MR1_Device Feature 1 (MA[7:0] = 01_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
1	01_H	Device Feature1	W	nWR (for AP)			(RFU)		BL		

Feature	Type	OP	Definition
BL	Write-only	OP<2:0>	**011_B:** BL8 (default) All others: reserved
nWR (for AP)	Write -only	OP<7:5>	If *n*WRE (MR2 OP<4>) = 0: **001_B**: *n*WR=3 (default) **100_B**: *n*WR=6 **110_B**: *n*WR=8 **111_B**: *n*WR=9 If *n*WRE (MR2 OP<4> = 1: **000_B**: *n*WR=10 **001_B**: *n*WR=11 **010_B**: *n*WR=12 All others: reserved

NOTE 1 Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

Burst Sequence

C2	C1	C0	BL	Burst Cycle Number and Burst Address Sequence							
				1	2	3	4	5	6	7	8
0_B	0_B	0_B	8	0	1	2	3	4	5	6	7
0_B	1_B	0_B		2	3	4	5	6	7	0	1
1_B	0_B	0_B		4	5	6	7	0	1	2	3
1_B	1_B	0_B		6	7	0	1	2	3	4	5

1. C0 input is not present on CA bus. It is implied zero.
2. The burst address represents C2 - C0.

MR2_Device Feature 2 (MA[7:0] = 02_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
2	02_H	Device Feature2	W	WRLev	WL Sel	(RFU)	nWRE	RL & WL			

Feature	Type	OP	Definition
RL & WL	Write-only	OP<3:0>	If OP<6> =0 (WL Set A, default) **0001B**: RL = 3 / WL = 1 (≦166 MHz) **0100B**: RL = 6 / WL = 3 (≦400 MHz) **0110B**: RL = 8 / WL = 4 (≦533 MHz) **0111B**: RL = 9 / WL = 5 (≦600 MHz) **1000B**: RL = 10 / WL = 6 (≦667 MHz, default) **1001B**: RL = 11 / WL = 6 (≦733 MHz) **1010B**: RL = 12 / WL = 6 (≦800 MHz) **1100B**: RL = 14 / WL = 8 (≦933 MHz) All others: reserved If OP<6> =1 (WL Set B) **0001B**: RL = 3 / WL = 1 (≦166 MHz) **0100B**: RL = 6 / WL = 3 (≦400 MHz) **0110B**: RL = 8 / WL = 4 (≦533 MHz) **0111B**: RL = 9 / WL = 5 (≦600 MHz) **1000B**: RL = 10 / WL = 8 (≦667 MHz) **1001B**: RL = 11 / WL = 9 (≦733 MHz) **1010B**: RL = 12 / WL = 9 (≦800 MHz) **1100B**: RL = 14 / WL = 11 (≦933 MHz) All others: reserved
nWRE	Write-only	OP<4>	**0B:** enable *n*WR programming ≦9 **1B:** enable *n*WR programming > 9 (default)
WL Selection	Write-only	OP<6>	**0B:** Select WL Set A (default) **1B:** Select WL Set B
WR Leveling	Write-only	OP<7>	**0B:** disabled (default) **1B:** enabled

NOTE 1 See MR0, OP<7>

NOTE 2 See MR0, OP<6>

MR3_I/O Configuration 1 (MA[7:0] = 03_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
3	03_H	I/O Config-1	W	(RFU)				DS			

Feature	Type	OP	Definition
Drive Strength	Write-only	OP<3:0>	**0000_B:** reserved **0001_B:** 34.3Ω typical **0010_B:** 40Ω typical (default) **0011_B:** 48Ω typical **0100_B:** 60Ω typical **0110_B:** 80Ω typical **1001_B:** 34.3Ω pull-down, 40Ω pull-up (240Ω termination) **1010_B:** 40Ω pull-down, 48Ω pull-up (240Ω termination) **1011_B:** 34.3Ω pull-down, 48Ω pull-up (120Ω termination) **All others:** reserved

MR4_Device Temperature (MA[7:0] = 04_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		

Feature	Type	OP	Definition
Refresh Rate	Read-only	OP<2:0>	**000B:** SDRAM Low temperature operating limit exceeded **001B:** 4x tREFI, 4x tREFIpb, 4x tREFW **010B:** 2x tREFI, 2x tREFIpb, 2x tREFW **011B:** 1x tREFI, 1x tREFIpb, 1x tREFW (≦85℃) **100B:** reserved **101B:** 0.25x tREFI, 0.25x tREFIpb, 0.25x tREFW, no AC timing derating **110B:** 0.25x tREFI, 0.25x tREFIpb, 0.25x tREFW, timing derating required **111B:** SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0B:** OP<2:0> value has not changed since last read of MR4. **1B:** OP<2:0> value has changed since last read of MR4.

NOTE 1 A mode register read from MR4 will reset OP7 to 0.

NOTE 2 OP7 is reset to 0 at power-up.

NOTE 3 If OP2 = 1, the device temperature is greater than 85˚C.

NOTE 4 OP7 is set to 1 if OP<2:0> has changed at any time since the last MR4 read.

NOTE 5 The device might not operate properly when OP<2:0> = 000b or 111b.

NOTE 6 For the specified operating temperature range and maximum operating temperature, refer to the Operating Temperature Range table.

NOTE 7 LPDDR3 devices must be derated by adding 1.875ns to the following core timing parameters:tRCD, tRC, tRAS, tRP, and tRRD. The tDQSCK parameter must be derated as specified in the AC Timing table. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.

NOTE 8 The recommended frequency for reading MR4 is provided in the Temperature Sensor section.

MR5_Basic Configuration-1 (MA[7:0] = 05_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
5	05_H	Basic Config-1	R	Manufacturer ID							

Feature	Type	OP	Definition
Manufactuer ID	Read-only	OP<7:0>	**0000 0101B:** Nanya **All Others:** Reserved

MR6_Basic Configuration-2 (MA[7:0] = 06_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
6	06_H	Basic Config-2	R	Revision ID1							

Feature	Type	OP	Definition
Revision ID1	Read-only	OP<7:0>	**0000 0000B:** A-die **All Others:** Reserved

MR7_Basic Configuration-3 (MA[7:0] = 07_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
7	07_H	Basic Config-3	R	Revision ID2							

Feature	Type	OP	Definition
Revision ID2	Read-only	OP<7:0>	**0000 0000B:** A Version **All Others:** Reserved

MR8_Basic Configuration-4 (MA[7:0] = 08H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
8	08_H	Basic Config-4	R	I/O width		Density				Type	

Feature	Type	OP	Definition
Type	Read-only	OP<1:0>	**11B:** LPDDR3 S8 **All others:** Reserved
Density	Read-only	OP<5:2>	**0110B:** 4Gb **0111B:** 8Gb **1000B:** 16Gb **1001B:** 32Gb **All others:** Reserved
I/O width	Read-only	OP<7:6>	**00B:** x32 **01B:** x16 **All others:** Reserved

NOTE 1 All the information is for die level.

MR9_Test Mode (MA<7:0> = 09H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
9	09_H	Test Mode	W	Vendor-Specific Test Mode							

MR10_Calibration (MA[7:0] = $0A_H$)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
10	$0A_H$	IO Calibration	W	Calibration Code							

Feature	Type	OP	Definition
Calibration Code	Write-only	OP<7:0>	**0xFF:** Calibration command after initialization **0xAB:** Long calibration **0x56:** Short calibration **0xC3:** ZQ Reset **All Others:** Reserved

NOTE 1 Host processor shall not write MR10 with “Reserved” values.

NOTE 2 The device ignores calibration commands when a reserved value is written into MR10.

NOTE 3 See AC Timing table for the calibration latency.

NOTE 4 If ZQ is connected to VSS through RZQ, either the ZQ calibration function (see MRW ZQ CALIBRATION Command) or default calibration (through the ZQ RESET command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration and ZQ CALIBRATION commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.

NOTE 5 Devices that do not support calibration ignore the ZQ CALIBRATION command.

NOTE 6 The MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR11_ODT (MA[7:0] = $0B_H$)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
11	$0B_H$	ODT	W	(RFU)					PD ctl	DQ ODT	

Feature	Type	OP	Definition
DQ ODT[1]	Write-only	OP<1:0>	**00B:** Disable (Default) **01B:** Reserved **10B:** *R*ZQ/2 **11B:** *R*ZQ/1
PD Control	Write-only	OP<2>	**0B:** ODT disabled by DRAM during power down (default) **1B:** ODT enabled by DRAM during power down

NOTE 1 Depending on ballout, ODT pin may be NOT supported so ODT die pad is connected to Vss inside the package.

MR12-15_Reserved (MA[7:0] = $0C_H$-$0F_H$)

MR16_PASR_BANK (MA[7:0] = 10_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10_H	PASR_BANK	W	PASR Bank Mask							

Feature	Type	OP	Definition
PASR Bank Mask	Write-only	OP<7:0>	**0B:** refresh enable to the bank (= unmasked, default) **1B:** refresh blocked (= masked)

OP	Bank Mask	LPDDR3 SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
4	XXX1XXXX	Bank 4
5	XX1XXXXX	Bank 5
6	X1XXXXXX	Bank 6
7	1XXXXXXX	Bank 7

MR17_PASR_Segment (MA[7:0] = 11_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
17	11_H	PASR_Seg	W	PASR Segment Mask							

Feature	Type	OP	Definition
PASR Segment Mask	Write-only	OP<7:0>	**0B:** refresh enable to the segment (=unmasked, default) **1B:** refresh blocked (=masked)

Segment	OP	Segment Mask	4Gb	8Gb	16Gb	32Gb
			R13:11	R14:12	R14:12	TBD
0	0	XXXXXXX1	000_B			
1	1	XXXXXX1X	001_B			
2	2	XXXXX1XX	010_B			
3	3	XXXX1XXX	011_B			
4	4	XXX1XXXX	100_B			
5	5	XX1XXXXX	101_B			
6	6	X1XXXXXX	110_B			
7	7	1XXXXXXX	111_B			

NOTE 1 This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.

NOTE 2 No memory present at addresses with R13=R14=HIGH. Segment masks 6 and 7 are ignored.

MR18-31_Reserved (MA[7:0] = 12_H.$1F_H$)

MR32_DQ Calibration Pattern A (MA[7:0] = 20_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	20_H	DQ calibration pattern A	R	See Data Calibration Pattern Description							

NOTE 1 Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration"

MR33-39_Do Not Use (MA[7:0] = 21_H-27_H)

MR40_DQ Calibration Pattern B (MA[7:0] = 28_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
40	28_H	DQ calibration pattern B	R	See Data Calibration Pattern Description							

NOTE 1 Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration"

MR41_CA Training 1 (MA[7:0] = 29_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
41	29_H	CA Training 1	W	See MRW – CA Training Mode							

NOTE 1 Writes to MR41 enables CA Training. See Mode Register Write - CA Training Mode

MR42_CA Training 2 (MA[7:0] = $2A_H$)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
42	$2A_H$	CA Training 2	W	See MRW – CA Training Mode							

NOTE 1 Writes to MR42 enables CA Training. See Mode Register Write - CA Training Mode

MR43-47_Do Not Use (MA[7:0] = $2B_H$-$2F_H$)

MR48_CA Training 3 (MA[7:0] = 30_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
48	30_H	CA Training 3	W	See MRW – CA Training Mode							

NOTE 1 Writes to MR48 enables CA Training. See Mode Register Write - CA Training Mode

MR49-62_Do Not Use (MA[7:0] = 31_H-$3E_H$)

MR63_RESET (MA[7:0] = $3F_H$)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
63	$3F_H$	RESET	W	X or 0xFCh							

MR64-255_Reserved (MA[7:0] = 40_H-FF_H)

LPDDR3 SDRAM Truth Table

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Command Truth Table

SDRAM command	Command Pins			CA pins										
	CKE		$\overline{CS}$	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
	CK(n-1)	CK(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	
			X	MA6	MA7	X								
Refresh (per bank)[11]	H	H	L	L	L	H	L	X						
			X	X										
Refresh (all bank)	H	H	L	L	L	H	H	X						
			X	X										
Enter Self Refresh	H	L	L	L	L	H	X							
	X		X	X										
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	
			X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	
			X	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	
			X	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	
Precharge (pre bank, all bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	
			X	X										
Enter Deep Power Down	H	L	L	H	H	L	X							
	X		X	X										
NOP	H	H	L	H	H	H	X							
			X	X										
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	X							
			X	X										
NOP	H	H	H	X										
			X	X										
Maintain PD, SREF, DPD (NOP)	L	L	H	X										
			X	X										
Enter Power Down	H	L	H	X										
	X		X	X										
Exit PD, SREF, DPD	L	H	H	X										
	X		X	X										

NOTE 1 All LPDDR3 commands are defined by states of $\overline{CS}$, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.

NOTE 3 AP "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.

NOTE 4 "X" means "H or L (but a defined logic level)", except when the LPDDR3 SDRAM is in PD, SREF, or DPD, in which case $\overline{CS}$, CK/$\overline{CK}$, and CA can be floated.

NOTE 5 Self refresh exit and Deep Power Down exit are asynchronous.

NOTE 6 *V*REF must be between 0 and *V*DDQ during Self Refresh and Deep Power Down operation.

NOTE 7 CAxr refers to command/address bit "x" on the rising edge of clock.

NOTE 8 CAxf refers to command/address bit "x" on the falling edge of clock.

NOTE 9 $\overline{CS}$ and CKE are sampled at the rising edge of clock.

NOTE 10 The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

NOTE 11 AB "high"during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

CKE Truth Table

Device Current State[3]	CKE_{n-1}[1]	CKE_n[1]	$\overline{CS}$[2]	Command n[4]	Operation n[4]	Device Next State	Notes
Active Power Down	L	L	x	x	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6,9
Idle Power Down	L	L	x	x	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6,9
Resetting Power Down	L	L	x	x	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6,9,12
Deep Power Down	L	L	x	x	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	x	x	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7,10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	13
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	13
	H	L	L	Enter DPD	Enter Deep Power Down	Deep Power Down	13
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
Other states	H	H	Refer to the Command Truth Table				

Notes:

1. "CKE_n" is the logic state of CKE at clock edge n; "CKE_{n-1}" was the logic state of CKE at previous clock edge.
2. "$\overline{CS}$" is the logic state of $\overline{CS}$ at the clock rising edge n;
3. "Current state" is the state of the LPDDR3 device immediately prior to clock edge n.
4. "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
5. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6. Power Down exit time (^tXP) should elapse before a command other than NOP is issued.
7. Self-Refresh exit time (^tXSR) should elapse before a command other than NOP is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the DPD section of the Functional Description.
9. The clock must toggle at least once during the ^tXP period.
10. The clock must toggle at least once during the ^tXSR period.
11. "X" means "Don't care".
12. Upon exiting Resetting Power Down, the device will return to the idle state if $^tINIT5$ has expired.
13. In the case of ODT disabled, all DQ output shall be Hi-Z. In the case of ODT enabled, all DQ shall be terminated to VDDQ.

State Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

Current State Bank n – Command to Bank n

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Banks)	Begin to refresh	Refreshing (All Banks)	7
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle / MR Reading	
	Reset	Begin Device Auto-initialization	Resetting	7,8
	Precharge	Deactivate row(s) in bank or banks	Precharging	9,15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row(s) in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10,11
	Write	Select column, and start write burst	Writing	10,11,12
Writing	Write	Select column, and start new write burst	Writing	10,11
	Read	Select column, and start read burst	Reading	10,11,13
Power On	MRW Reset	Begin Device Auto-initialization	Resetting	7,9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1. The table applies when both CKE_{n-1} and CKE_n are HIGH, and after ^tXSR or ^tXP has been met, if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State definitions:

State	Definition
Idle	The bank or banks have been precharged, and tRP has been met.
Active	A row in the bank has been activated, and tRCD has been met. No data bursts or accesses and no register accesses are in progress.
Reading	A READ burst has been initiated with auto precharge disabled, and has not yet terminated.
Writing	A WRITE burst has been initiated with auto precharge disabled, and has not yet terminated.

4. The following states must not be interrupted by any executable command. NOP commands must be applied to each positive clock edge during these states.

State	Starts with	Ends when It's met	Notes
Refreshing (per bank)	Registration of a REFRESH (per bank) command	tRFCpb	After tRFCpb is met, the bank is in the idle state.
Refreshing (all banks)	Registration of a REFRESH (all bank) command	tRFCab	After tRFCab is met, the device is in the all-banks idle state.
Idle MR reading	Registration of the MRR command	tMRR	After tMRR is met, the device is in the all-banks idle state..
Resetting MR reading	Registration of the MRR command	tMRR	After tMRR is met, the device is in the all-banks idle state.
Active MR reading	Registration of the MRR command	tMRR	After tMRR is met, the bank is in the active state.
MR writing	Registration of the MRW command	tMRW	After tMRW is met, the device is in the all-banks idle state.
Precharging all	Registration of a PRECHARGE ALL command	tRP	After tRP is met, the device is in the all-banks idle state.

5. The states listed below must not be interrupted by a command issued to the same command. NOP commands or supported commands to the other bank should be issued on any clock edge occurring during these states.

State	Starts with	Ends when It's met	Notes
Precharging	Registration of a PRECHARGE command	tRP	After tRP is met, the bank is in the idle state.
Row Activing	Registration of an ACTIVATE command	tRCD	After tRCD is met, the bank is in the active state.
READ with AP enabled	Registration of a READ command with auto precharge enabled	tRP	After tRP is met, the bank is in the idle state.
WRITE with AP enabled	Registration of a WRITE command with auto precharge enabled	tRP	After tRP is met, the bank is in the idle state.

6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific reset command is achieved through Mode Register Write command.
9. This command may or may not be bank specific. If all banks are being precharged, the must be in a valid state for precharging.
10. A command other than NOP should not be issued to the same bank while a READ or WRITE burst with auto precharge is enabled.
11. The new READ or WRITE command could be auto precharge enabled or auto precharge disabled.
12. A WRITE command can be issued after the completion of the READ burst.
13. A READ command can be issued after completion of the WRITE burst.
14. If a PRECHARGE command is issued to a bank in the idle state, tRP still applies.

Current State Bank n – Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	Notes
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command supported to Bank m	-	
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	6
	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7
	Precharge	Deactivate row(s) in bank or banks	Precharging	8
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	9,10,11
Reading (AP disabled)	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7,12
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row(s) in bank or banks	Precharging	8
Writing (AP disabled)	Read	Select column, and start read burst from Bank m	Reading	7,13
	Write	Select column, and start write burst to Bank m	Writing	7
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row(s) in bank or banks	Precharging	8
Reading with Auto-Precharge	Read	Select column, and start read burst from Bank m	Reading	7,14
	Write	Select column, and start write burst to Bank m	Writing	7,12,14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row(s) in bank or banks	Precharging	8
Writing with Auto-Precharge	Read	Select column, and start read burst from Bank m	Reading	7,13,14
	Write	Select column, and start write burst to Bank m	Writing	7,14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row(s) in bank or banks	Precharging	8
Power On	MRW Reset	Begin Device Auto-initialization	Resetting	15,16
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1. This table applies when:
   1a. the previous state was self refresh or power-down
   1b. after tXSR or tXP has been met
   1c. and both CKEn -1 and CKEn are HIGH
2. All states and sequences not shown are illegal or reserved.
3. Current state definitions:

State	Condition	And…	And…
Idle	The bank has been precharged	tRP is met	
Active	A row in the bank has been activated	tRCD is met	No data bursts/accesses and no register accesses are in progress.
Reading	A READ burst has been initiated with auto precharge disabled	The READ has not yet terminated.	
Writing	A WRITE burst has been initiated with auto precharge disabled	The WRITE has not yet terminated.	

4. Refresh, self refresh, and MRW commands can only be issued when all banks are idle.

5. The states listed below must not be interrupted by any executable command. NOP commands must be applied during each clock cycle while in these states:

State	Starts with:	Ends when:	Notes
Idle MR reading	Registration of the MRR command	*t*MRR is met	After *t*MRR is met, the device is in the all-banks idle state.
Resetting MR reading	Registration of the MRR command	*t*MRR is met	After *t*MRR is met, the device is in the all-banks idle state.
Active MR reading	Registration of the MRR command	*t*MRR is met	After *t*MRR is met, the bank is in the active state.
MR writing	Registration of the MRW command	*t*MRW is met	After *t*MRW is met, the device is in the all-banks idle state.

6. tRRD must be met between the ACTIVATE command to bank n and any subsequent ACTIVATE command to bank m.
7. READs or WRITEs listed in the command column include READs and WRITEs with or without auto precharge enabled.
8. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
9. MRR is supported in the row-activating state.
10. MRR is supported in the precharging state.
11. The next state for bank m depends on the current state of bank m (idle, row-activating, precharging, or active).
12. A WRITE command can be issued only after the completion of the READ burst
13. A READ command can be issued only after the completion of the WRITE burst.
14. A READ with auto precharge enabled or a WRITE with auto precharge enabled can be followed by any valid command to other banks provided that the timing restrictions are met.
15. Not bank-specific; requires that all banks are idle and no bursts are in progress.
16. RESET command is achieved through MODE REGISTER WRITE command.

DM Operation Truth Table

The DM truth table provides specifications for data masking.

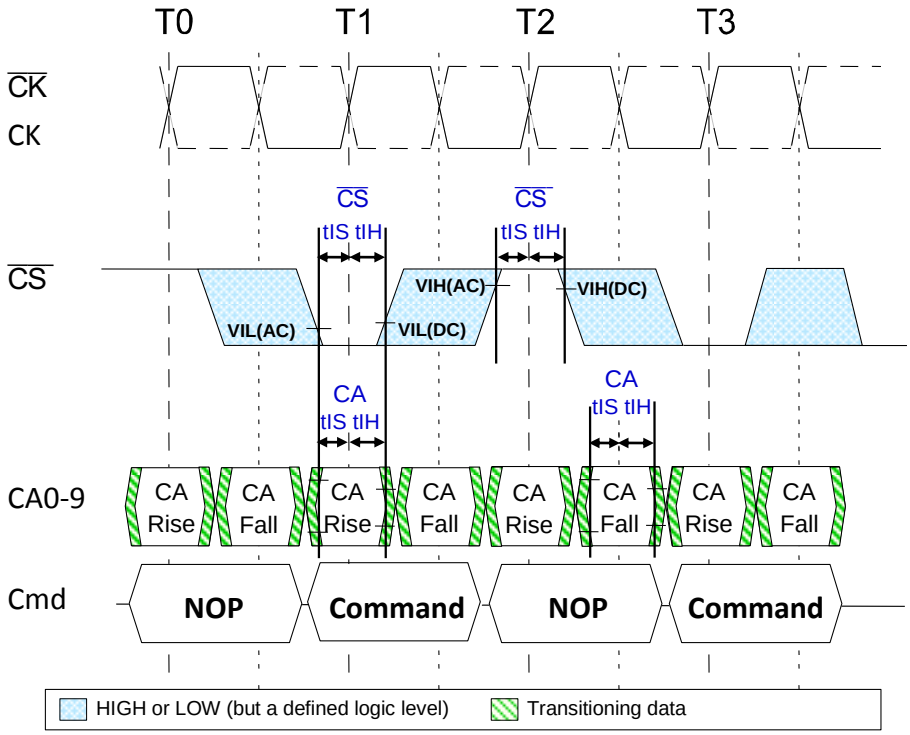
DM Truth Table

Function	DM	DQ	Notes
Write Enable	L	Valid	1
Write Inhibit	H	x	1

Note: Used to mask write data, provided simultaneouslywith the corresponding input data.

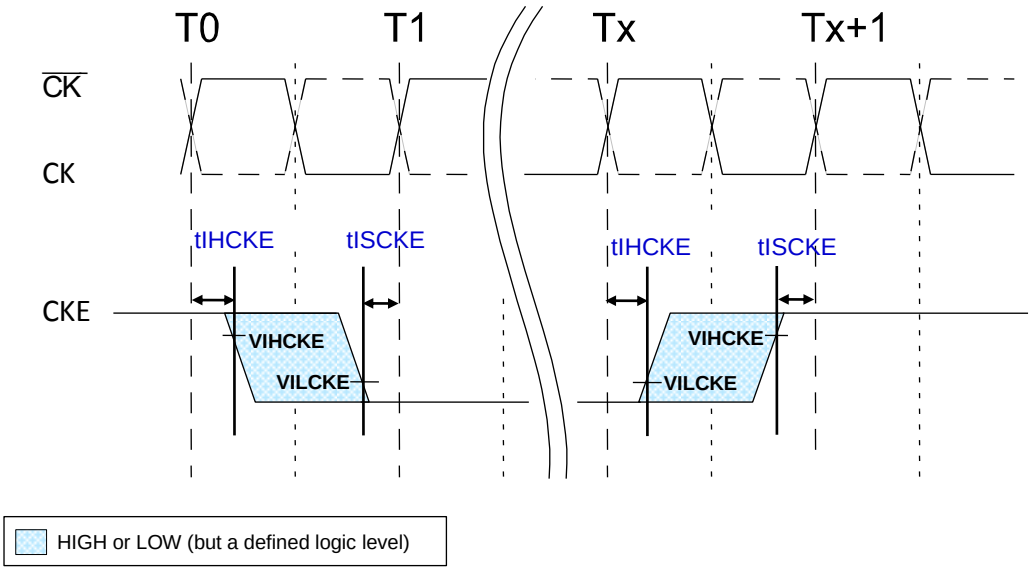
Commands and Timing

Command Input Setup and Hold



NOTE 1 Setup and hold conditions also apply to the CKE pin. For timing diagrams related to the CKE pin, see “Power-Down”

CKE Input Setup and Hold



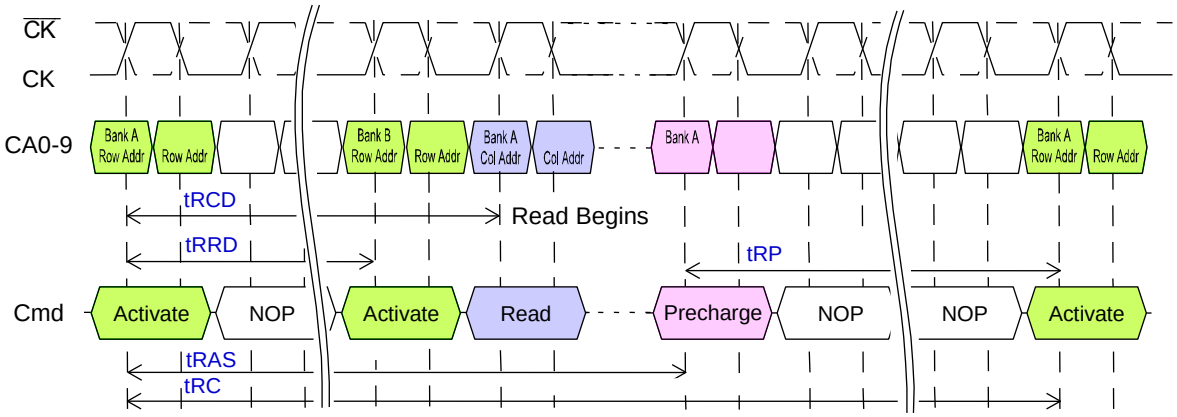
NOTE 1 After CKE is registered LOW, CKE signal level shall be maintained below VILCKE for tCKE specification (LOW pulse width).

NOTE 2 After CKE is registered HIGH, CKE signal level shall be maintained above VIHCKE for tCKE specification (HIGH pulse width).

ACTIVE

The ACTIVATE command is issued by holding $\overline{CS}$ LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 to BA2 are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at tRCD after the ACTIVATE command is issued. After a bank has been activated it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between ACTIVATE commands to different banks is tRRD.

ACTIVATE Command



NOTE 1 A PRECHARGE-all command uses tRPab timing, while a single-bank PRECHARGE command uses tRPpb timing. In this figure, tRP is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE.

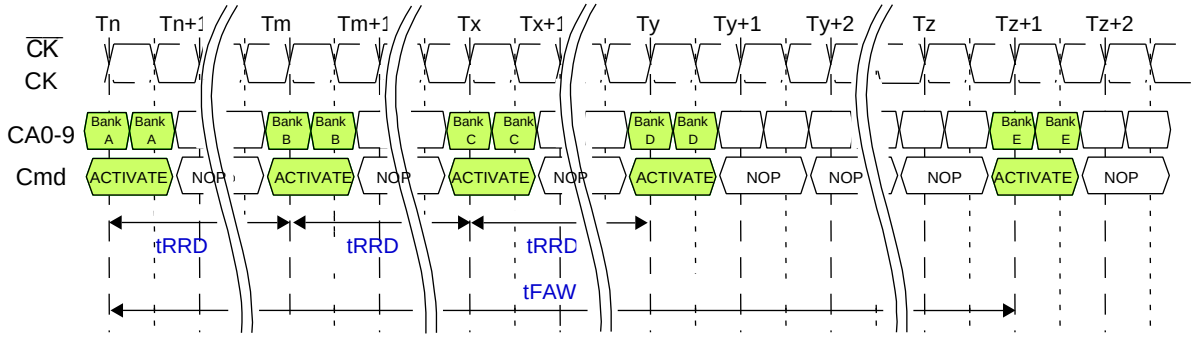
8-Bank Device Operation

Certain restrictions on operation of the 8-bank devices must be observed. There are two rules: One rule restricts the number of sequential ACTIVATE commands that can be issued; the other provides more time for RAS precharge for a PRECHARGE ALL command. The rules are as follows:

The 8-Bank Device Sequential Bank Activation Restriction: No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling *t*FAW window. The number of clocks in a *t*FAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting to clocks is done by dividing *t*FAW[ns] by *t*CK[ns], and rounding up to the next integer value. As an example of the rolling window, if RU(*t*FAW/*t*CK) is 10 clocks, and an ACTIVATE command is issued in clock *n*, no more than three further ACTIVATE commands can be issued at or between clock *n* + 1 and *n* + 9. REFpb also counts as bank activation for purposes of *t*FAW. If the clock frequency is changed during the *t*FAW period, the rolling *t*FAW window may be calculated in clock cycles by adding up the time spent in each clock period. The *t*FAW requirement is met when the previous *n* clock cycles exceeds the *t*FAW time.

The 8-Bank Device Precharge-All Allowance: *t*RP for a PRECHRGE ALL command must equal *t*RPab, which is greater than *t*RPpb.

tFAW Timing



READ and WRITE Access Modes

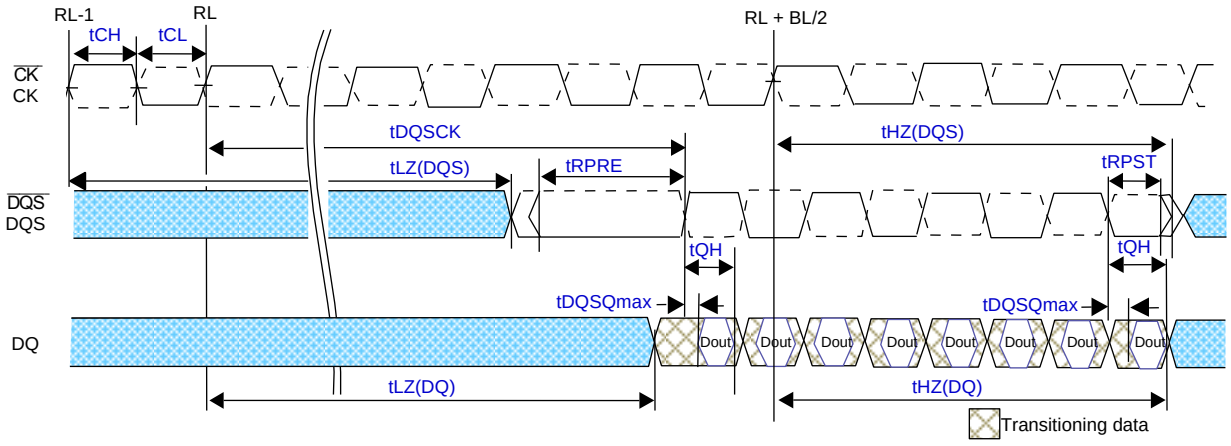
After a bank is activated, a READ or WRITE command can be issued with $\overline{CS}$ LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW).

The LPDDR3 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles. Burst interrupts are not allowed.

Burst READ

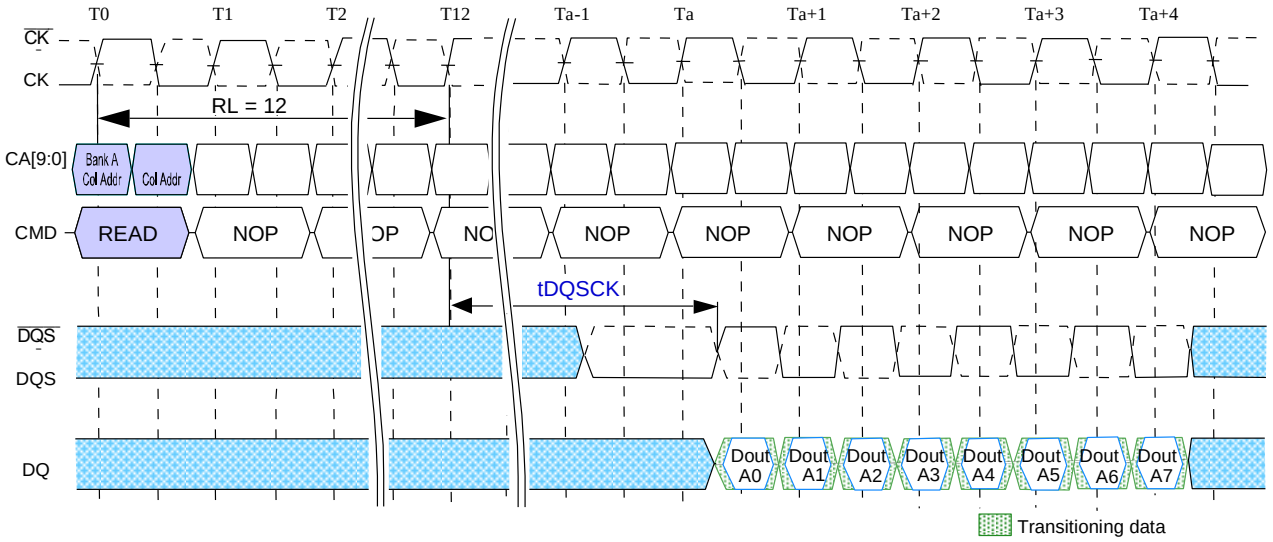
The burst READ command is initiated with $\overline{CS}$ LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs CA5r–CA6r and CA1f–CA9f determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available RL × *t*CK + *t*DQSCK + *t*DQSQ after the rising edge of the clock when the READ command is issued. The data strobe output is driven LOW *t*RPRE before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$.

READ Output Timing

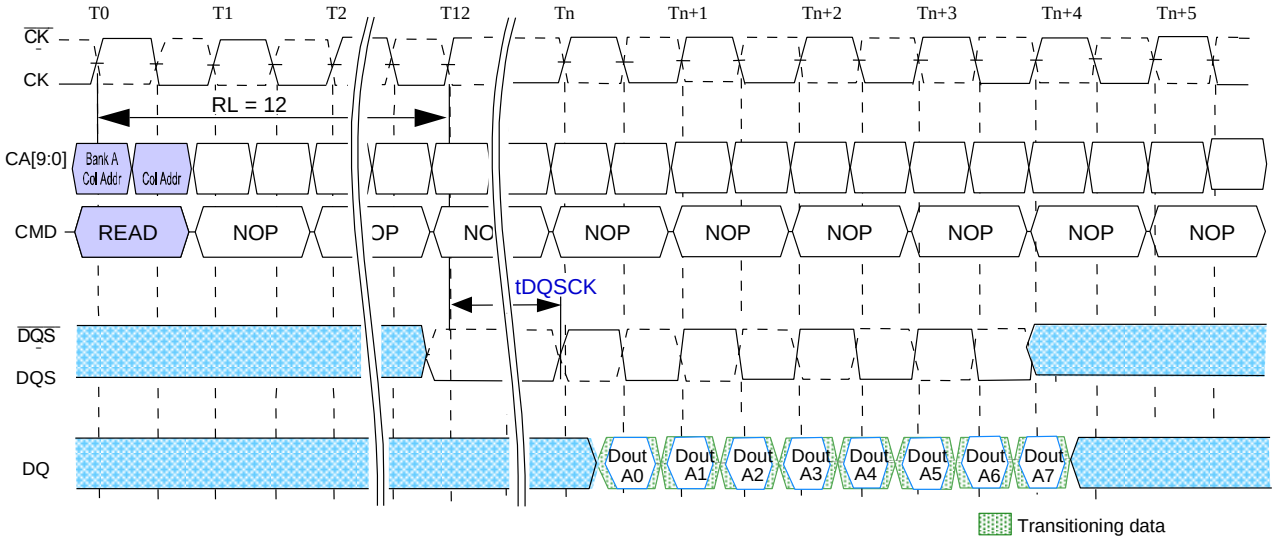


NOTE 1 tDQSCK can span multiple clock periods.

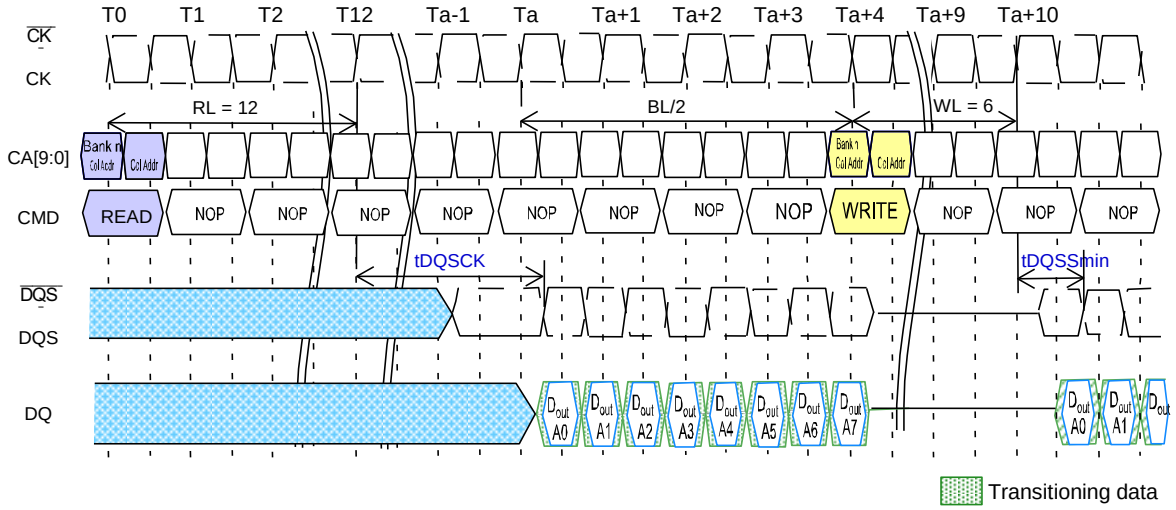
Burst READ: RL = 12, BL = 8, *t*DQSCK > *t*CK



Burst Read: RL = 12, BL = 8, *t*DQSCK < *t*CK

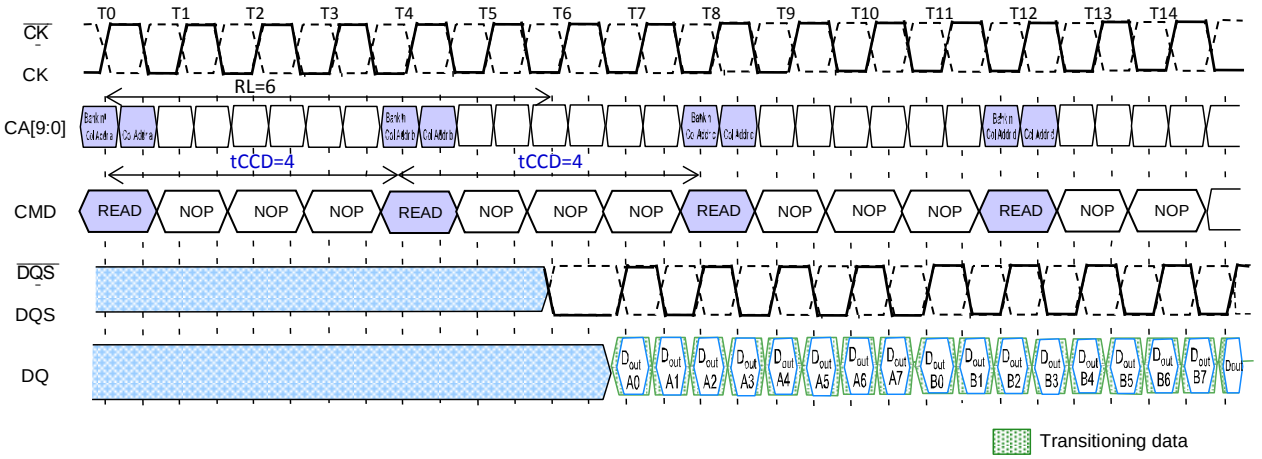


Burst READ Followed by Burst WRITE: RL = 12, WL = 6, BL = 8



The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(*t*DQSCK(MAX)/*t*CK) + BL/2 + 1 - WL clock cycles.

Seamless Burst READ – RL = 6, BL = 8, tCCD = 4

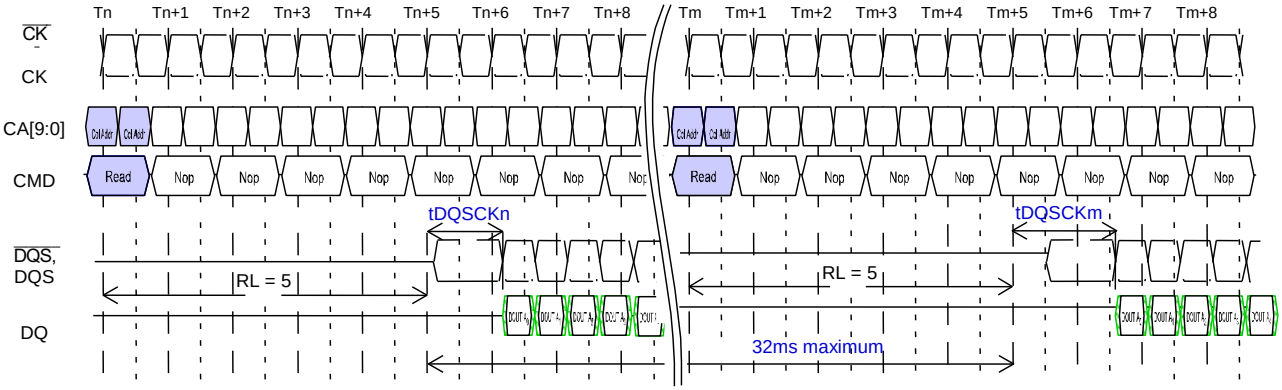


The seamless burst READ operation is supported by enabling a READ command at every fourth clock cycle for BL = 8 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

tDQSCK Delta Timing

In order to allow for the system to track variations in *t*DQSCK output across multiple clock cycles, three parameters, *t*DQSCKDS (delta short), *t*DQSCKDM (delta medium), and *t*DQSCKDL (delta long) are provided. Each of these parameters defines the change in *t*DQSCK over a short, medium, or long rolling window, respectively. The definitions for each *t*DQSCK-delta parameter show up on the next page.

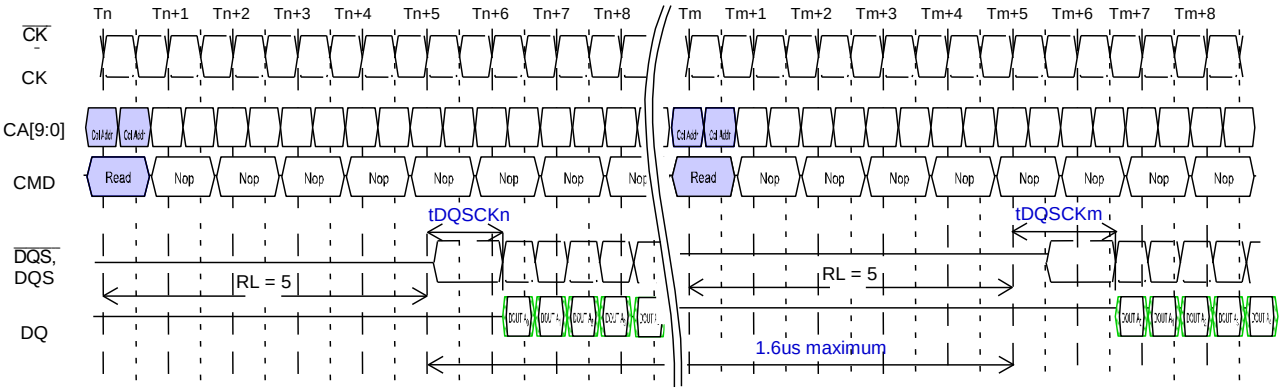
tDQSCKDL Timing



NOTE 1 tDQSCKDL = (tDQSCKn - tDQSCKm).

NOTE 2 tDQSCKDL,MAX is defined as the maximum of ABS (tDQSCKn - tDQSCKm) for any (tDQSCKn, tDQSCKm) pair within any 32ms rolling window.

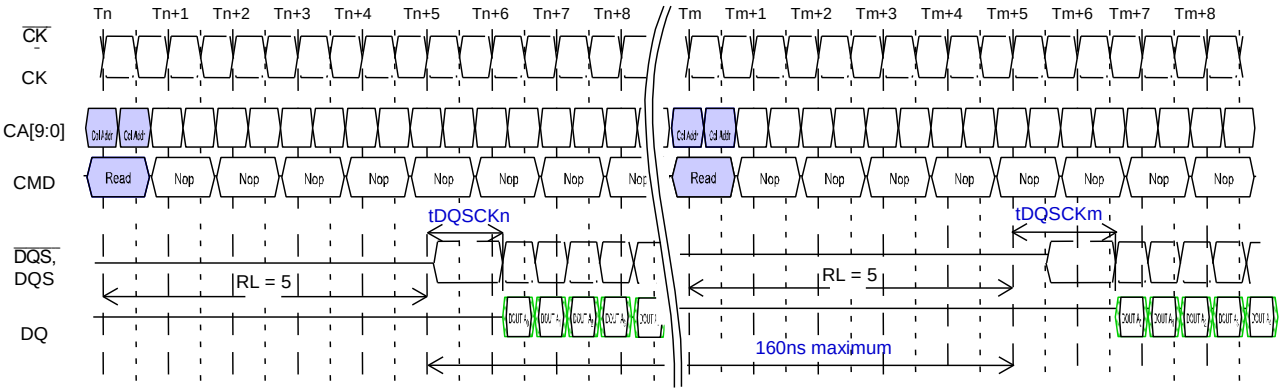
tDQSCKDM Timing



NOTE 1 tDQSCKDM = (tDQSCKn - tDQSCKm).

NOTE 2 tDQSCKDM,MAX is defined as the maximum of ABS (tDQSCKn - tDQSCKm) for any (tDQSCKn, tDQSCKm) pair within any 1.6µs rolling window.

tDQSCKDS Timing



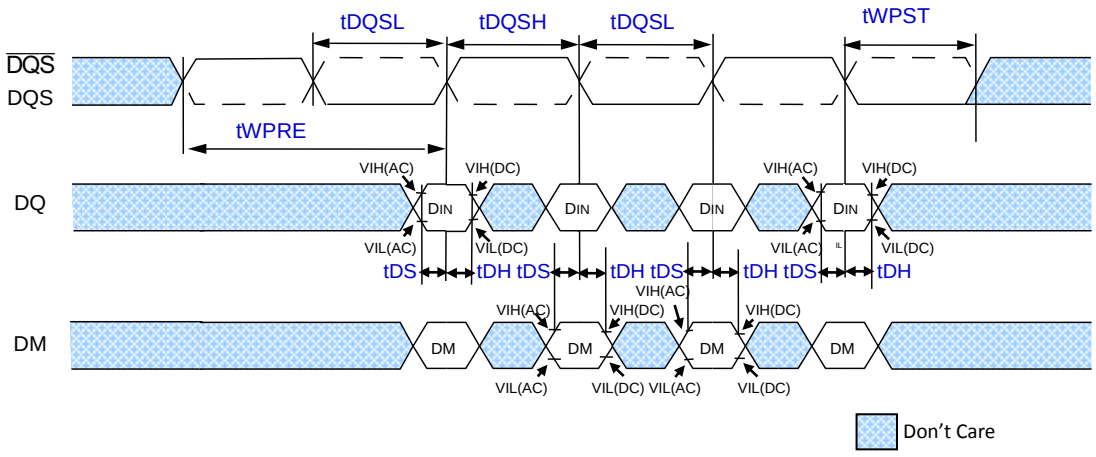
NOTE 1 tDQSCKDS = (tDQSCKn - tDQSCKm).

NOTE 2 tDQSCKDS,MAX is defined as the maximum of ABS (tDQSCKn - tDQSCKm) for any (tDQSCKn, tDQSCKm) pair for READs within a consecutive burst, within any 160ns rolling window.

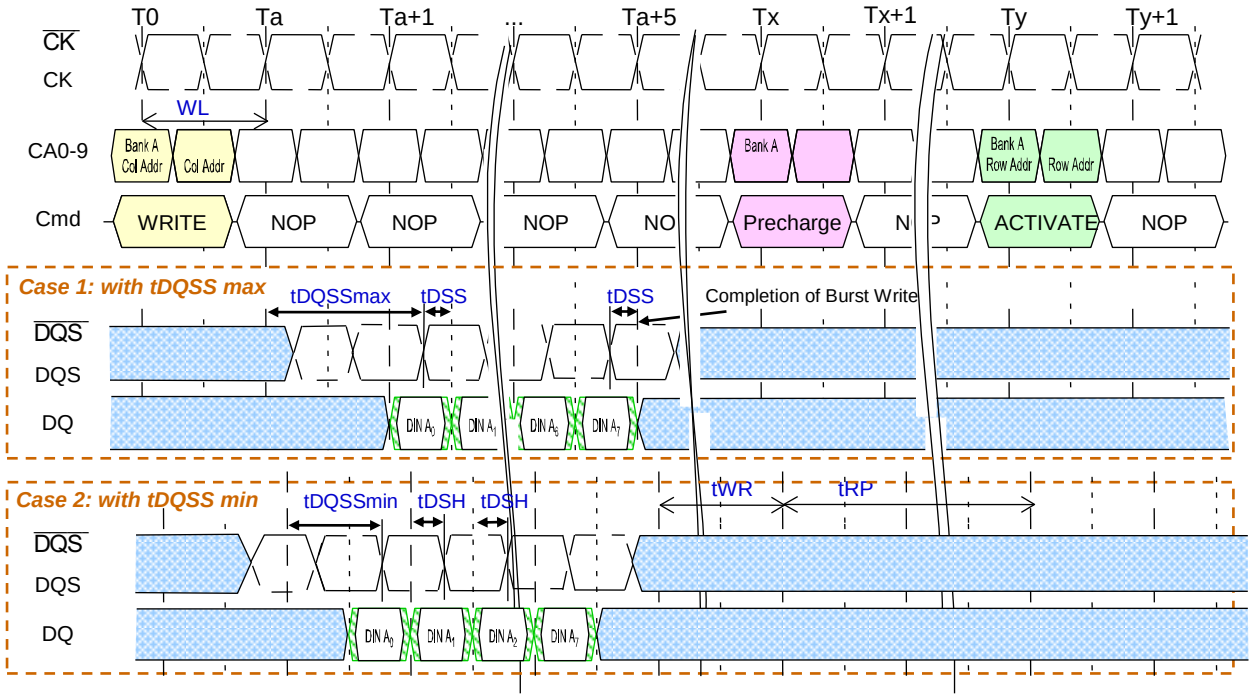
Burst WRITE

The burst WRITE command is initiated with $\overline{CS}$ LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the *t*DQSS delay is measured. The first valid data must be driven WL × *t*CK + *t*DQSS from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS) must be driven LOW *t*WPRE prior to data input. The burst cycle data bits must be applied to the DQ pins *t*DS prior to the associated edge of the DQS and held valid until *t*DH after that edge. Burst data is sampled on successive edges of the DQS until the burst is completed. After a burst WRITE operation, *t*WR must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$.

Data Input (WRITE) Timing



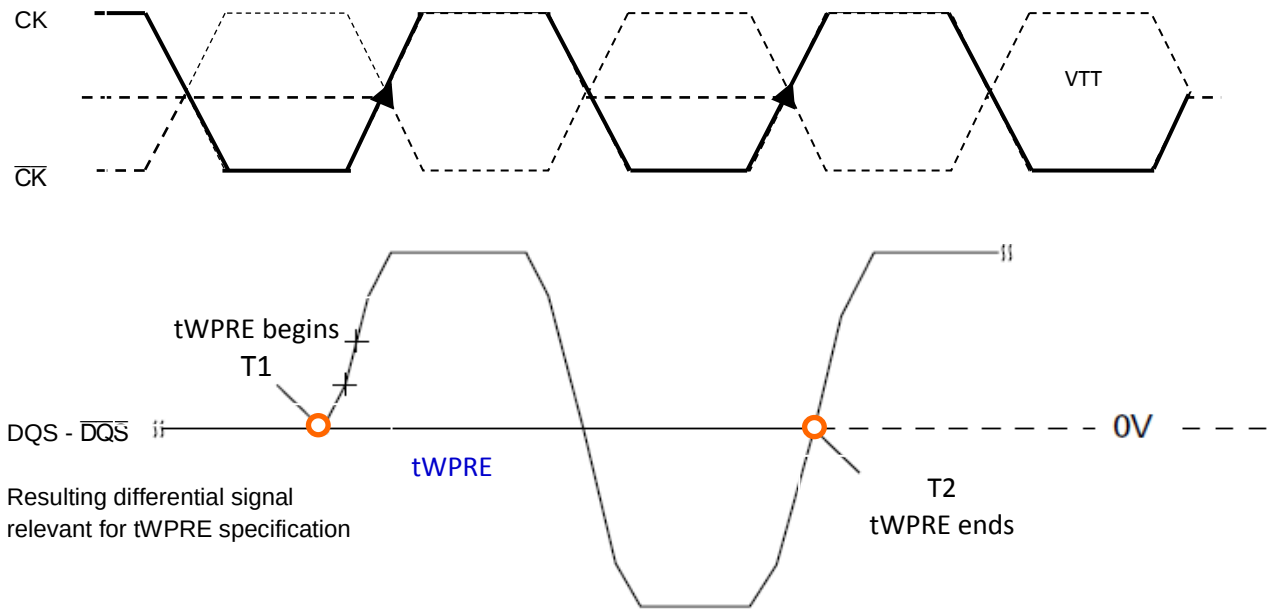
Burst WRITE



tWPRE Calculation

The method for calculating *t*WPRE is shown in the following figure:

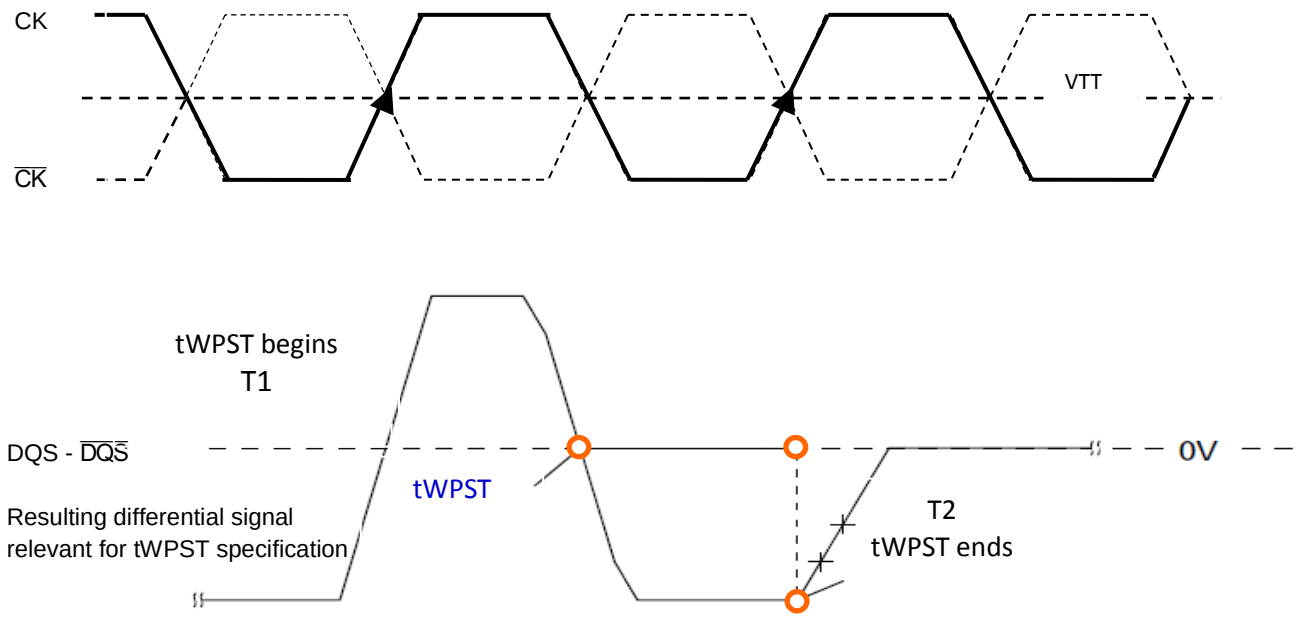
Method for Calculating *t*WPRE Transitions and Endpoints



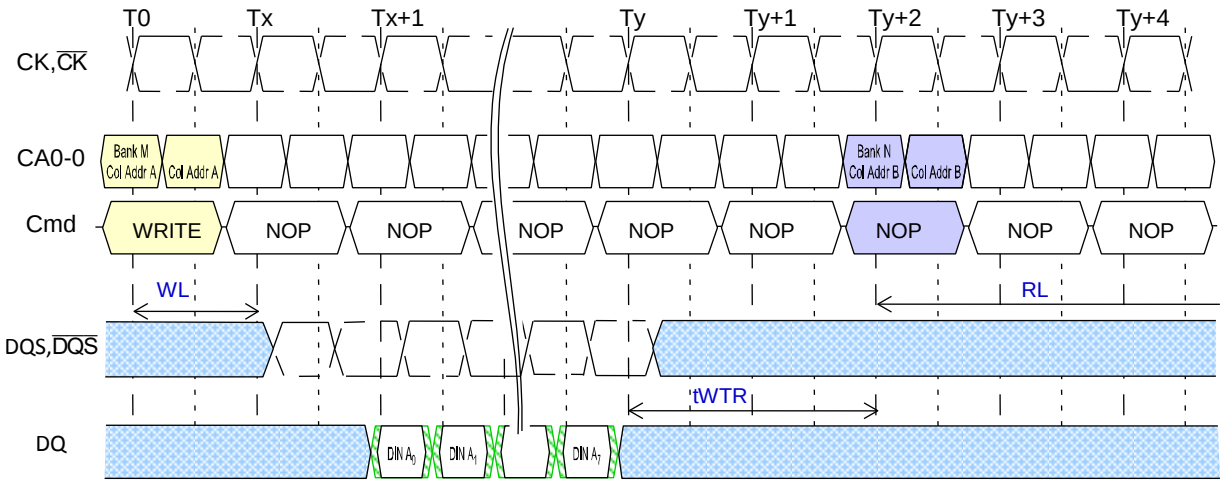
tWPST Calculation

The method for calculating tWPST is shown in the follwing figure:

Method for Calculating *t*WPST Transitions and Endpoints



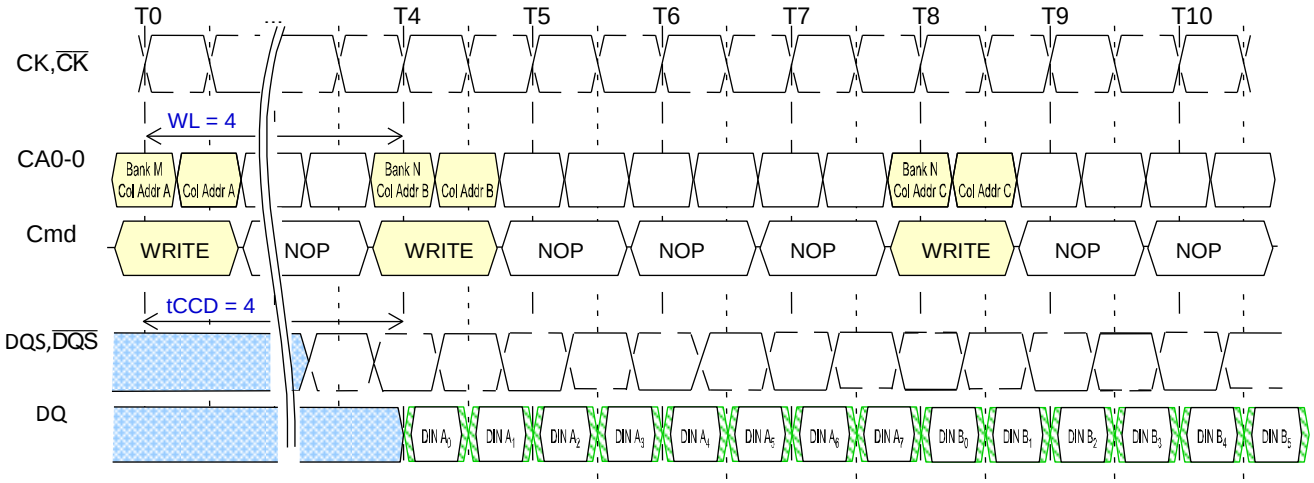
Burst WRITE Followed by Burst READ



NOTE 1 The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is [WL + 1 + BL/2 + RU(tWTR/tCK)].

NOTE 2 tWTR starts at the rising edge of the clock after the last valid input data.

Seamless Burst WRITE: WL = 4, BL = 8, *t*CCD = 4

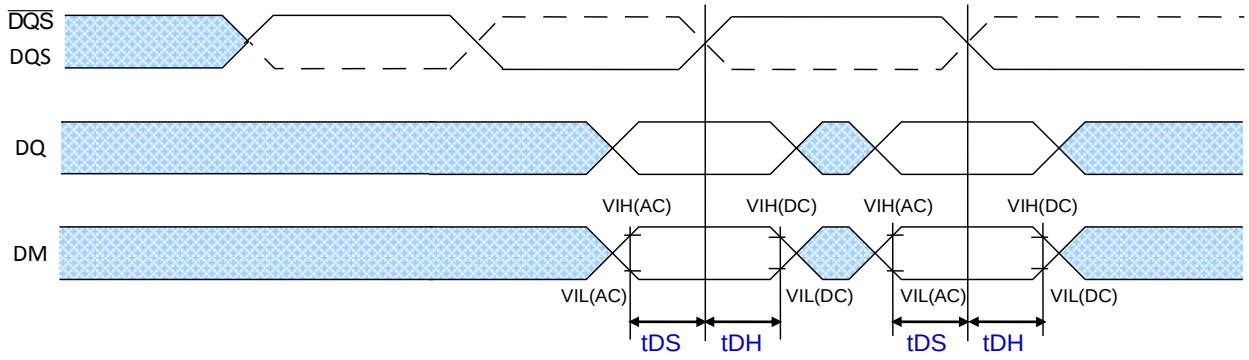


NOTE 1 The seamless burst WRITE operation is supported by enabling a write command every four clocks for BL = 8 operation. This operation is supported for any activated bank.

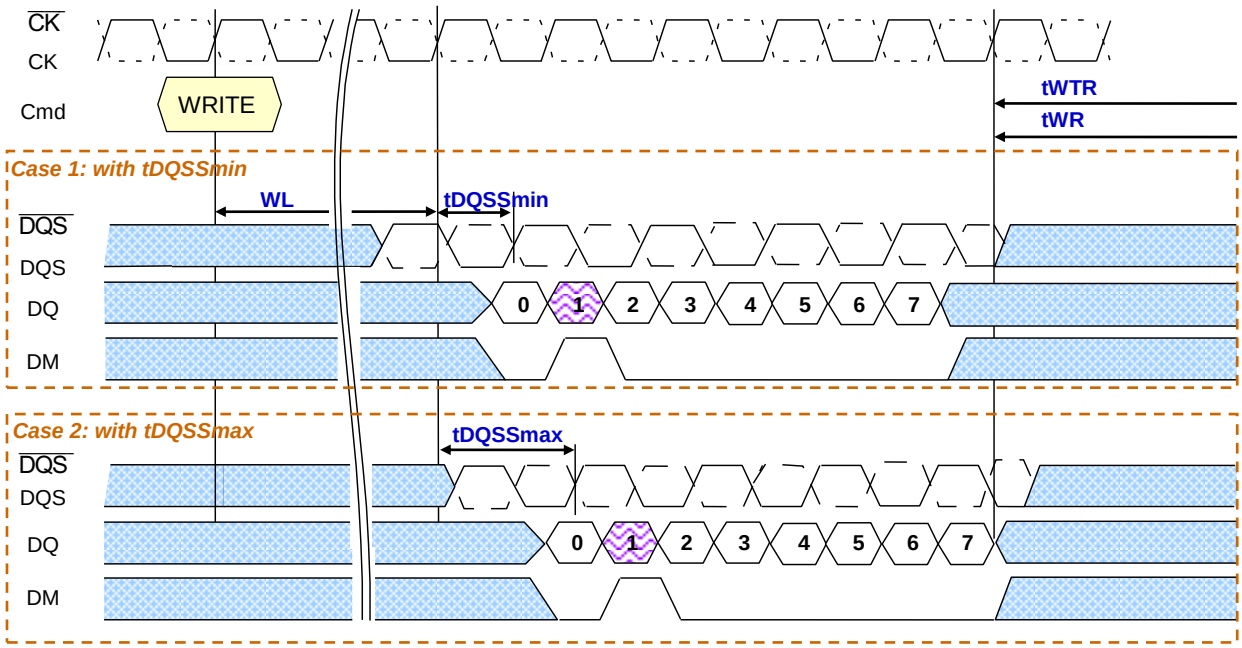
Write Data Mask

On LPDDR3 devices, one write data mask (DM) pin for each data byte (DQ) is supported, consistent with the implementation on LPDDR2 SDRAM. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing, but are inputs only. Internal data-mask loading is identical to data-bit loading to ensure matched system timing.

Data Mask Timing



WRITE Data Mask, Second Data Bit Masked



NOTE 1 For the data mask function, BL = 8 is shown; the second data bit is masked.

PRECHARGE Operation

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with $\overline{CS}$ LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bits BA0, BA1, and BA2 are used to determine which bank(s) to precharge.

The precharged bank(s) will be available for subsequent row access *t*RPab after an allbank PRECHARGE command is issued, or *t*RPpb after a single-bank PRECHARGE command is issued.

To ensure that LPDDR3 devices can meet the instantaneous current demand required to operate, the row-precharge time for an all-bank PRECHARGE (*t*RPab) will be longer than the row PRECHARGE time for a single-bank PRECHARGE (*t*RPpb).

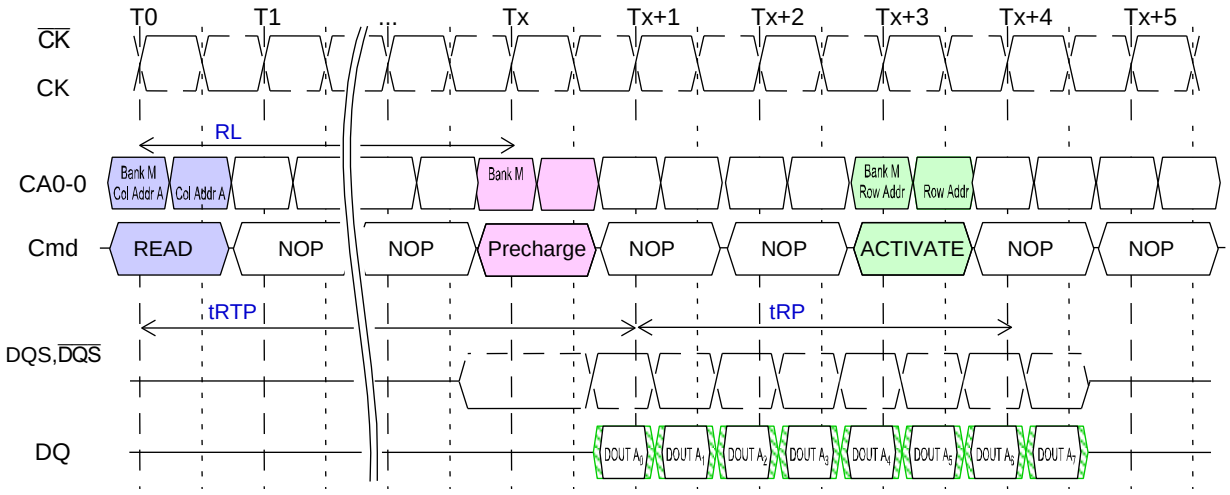
Bank Selection for PRECHARGE by Address Bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 8-bank device
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	Don't care	Don't care	Don't care	All Banks

Burst READ Operation Followed by PRECHARGE

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row PRECHARGE time (*t*RP) has elapsed. A PRECHARGE command cannot be issued until after *t*RAS is satisfied. For LPDDR3 devices, the minimum READ-to-PRECHARGE time (*t*RTP) must also satisfy a minimum analog time from the rising clock edge that initiates the last 8-bit prefetch of a READ command. *t*RTP begins BL/2 – 4 clock cycles after the READ command.

Burst READ Followed by PRECHARGE: BL = 8, RU(*t*RTP(MIN)/*t*CK) = 2

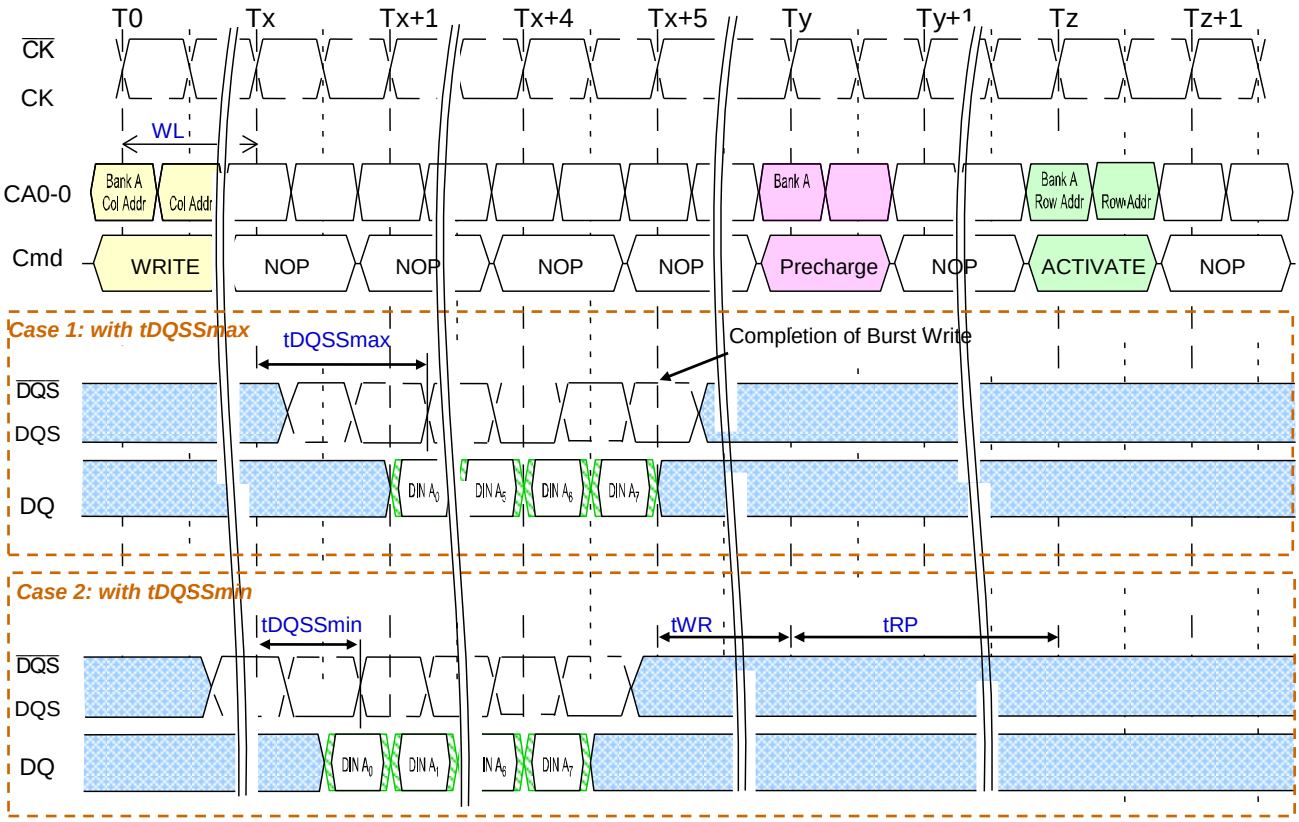


Burst WRITE Followed by PRECHARGE

For WRITE cycles, a WRITE recovery time (*t*WR) must be provided before a PRECHARGE command can be issued. This delay is referenced from the last valid burst input data to the completion of the burst WRITE. PRECHARGE command must not be issued prior to the *t*WR delay.

LPDDR3 devices write data to the array in prefetch multiples (prefetch = 8). An internal WRITE operation can only begin after a prefetch group has been completely latched, so *t*WR starts at prefetch boundaries. The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(*t*WR/*t*CK) clock cycles.

Burst WRITE Followed by PRECHARGE: BL = 8



Auto PRECHARGE Operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or a WRITE command is issued to the device, the AP bit (CA0f) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency) thus improving system performance for random data access.

Burst READ with Auto PRECHARGE

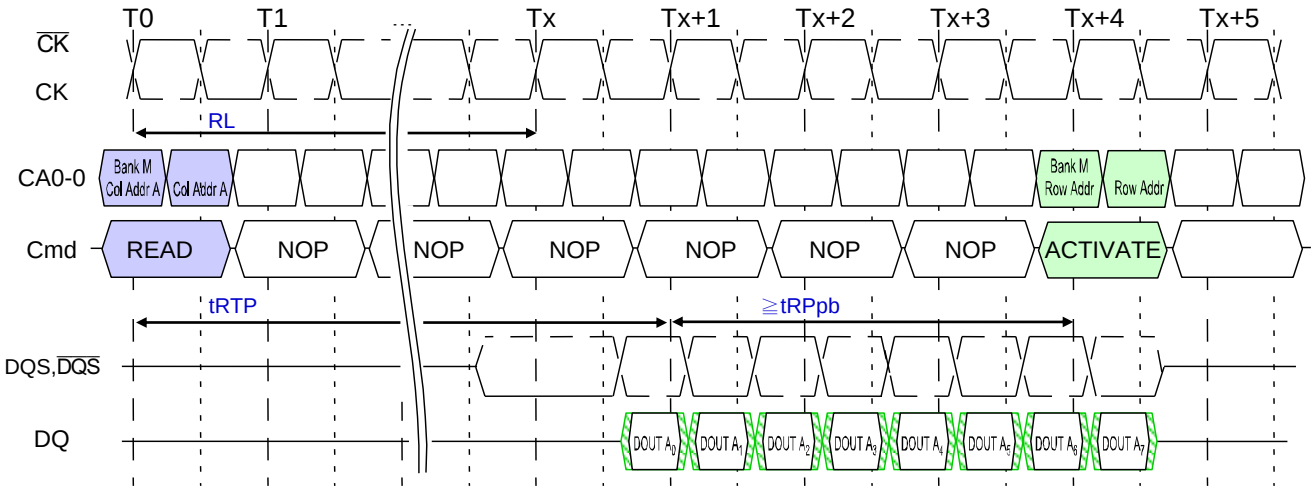
If AP (CA0f) is HIGH when a READ command is issued, the READ with auto-precharge function is engaged. LPDDR3 devices start an auto-precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(*t*RTP/*t*CK) clock cycles later than the READ with auto precharge command, whichever is greater.

Following an auto-precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:

• The RAS precharge time (*t*RP) has been satisfied from the clock at which the auto-precharge begins.

• The RAS cycle time (*t*RC) from the previous bank activation has been satisfied.

Burst READ with Auto Precharge: BL = 8, RU(*t*RTP(MIN)/*t*CK) = 4



Burst WRITE with Auto Precharge

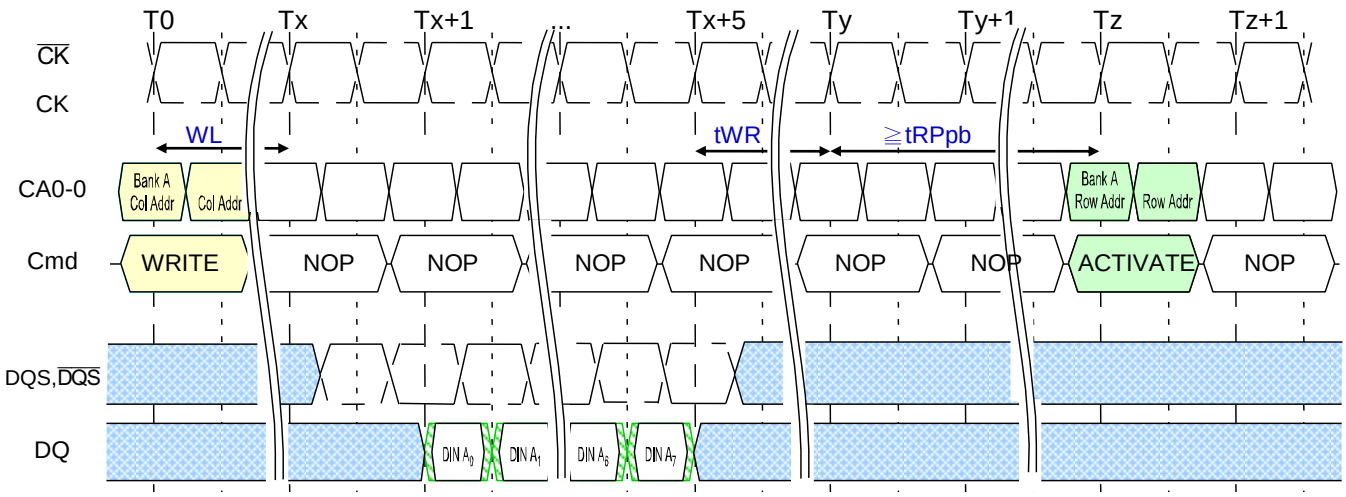
If AP (CA0f) is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge on the rising edge *t*WR cycles after the completion of the burst WRITE.

Following a WRITE with auto precharge, an ACTIVATE command can be issued to the same bank if the following two conditions are met:

• The RAS precharge time (*t*RP) has been satisfied from the clock at which the autoprecharge begins.

• The RAS cycle time (*t*RC) from the previous bank activation has been satisfied.

Burst WRITE with Auto Precharge: BL = 8



PRECHARGE and Auto Precharge Clarification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Notes
Read	Precharge (to same Bank as Read)	BL/2 + max(4, RU(tRTP/tCK)) - 4	tCK	1
	Precharge All	BL/2 + max(4, RU(tRTP/tCK)) - 4	tCK	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(4, RU(tRTP/tCK)) - 4	tCK	1,2
	Precharge All	BL/2 + max(4, RU(tRTP/tCK)) - 4	tCK	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(4, RU(tRTP/tCK)) - 4 + RU(tRPpb/tCK)	tCK	1
	Write or Write w/AP (same bank)	illegal	tCK	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU(tDQSCKmax/tCK) - WL + 1	tCK	3
	Read or Read w/AP (same bank)	illegal	tCK	3
	Read or Read w/AP (different bank)	BL/2	tCK	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU(tWR/tCK) + 1	tCK	1
	Precharge All	WL + BL/2 + RU(tWR/tCK) + 1	tCK	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + RU(tWR/tCK) + 1	tCK	1,2
	Precharge All	WL + BL/2 + RU(tWR/tCK) + 1	tCK	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU(tWR/tCK) + 1 + RU(tRPpb/tCK)	tCK	1
	Write or Write w/AP (same bank)	illegal	tCK	3
	Write or Write w/AP (different bank)	BL/2	tCK	3
	Read or Read w/AP (same bank)	illegal	tCK	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(tWTR/tCK) + 1	tCK	3
Precharge	Precharge (to same Bank as Precharge)	1	tCK	1
	Precharge All	1	tCK	1
Precharge All	Precharge	1	tCK	1
	Precharge All	1	tCK	1

Notes:

1. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after ^{t}RP depending on the latest precharge command issued to that bank.
2. Any command issued during the minimum delay time as specified above table is illegal.
3. After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write a/AP may not be interrupted or truncated.

REFRESH Command

The REFRESH command is initiated with $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. Per-bank REFRESH is initiated with CA3 LOW at the rising edge of the clock. All-bank REFRESH is initiated with CA3 HIGH at the rising edge of the clock.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device. The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin: 0-1-2-3-4-5-6-7-0-1-.... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh. Bank addressing for the per-bank REFRESH count is the same as established for the single-bank PRECHARGE command. A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions are met:

- tRFCab has been satisfied after the prior REFab command
- tRFCpb has been satisfied after the prior REFpb command
- tRP has been satisfied after the prior PRECHARGE command to that bank
- tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank is inaccessible during per-bank REFRESH cycle time (*t*RFCpb), however, other banks within the device are accessible and can be addressed during the cycle.During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, these conditions must be met:

- tRFCpb must be satisfied before issuing a REFab command
- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- tRRD must be satisfied before issuing an ACTIVATE command to a different bank
- tRFCpb must be satisfied before issuing another REFpb command.

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-all command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied following the prior REFab command
- tRFCpb has been satisfied following the prior REFpb command
- tRP has been satisfied following the prior PRECHARGE commands.

When an all-bank refresh cycle has completed, all banks will be idle. After issuing REFab:

- tRFCab latency must be satisfied before issuing an ACTIVATE command
- tRFCab latency must be satisfied before issuing a REFab or REFpb command.

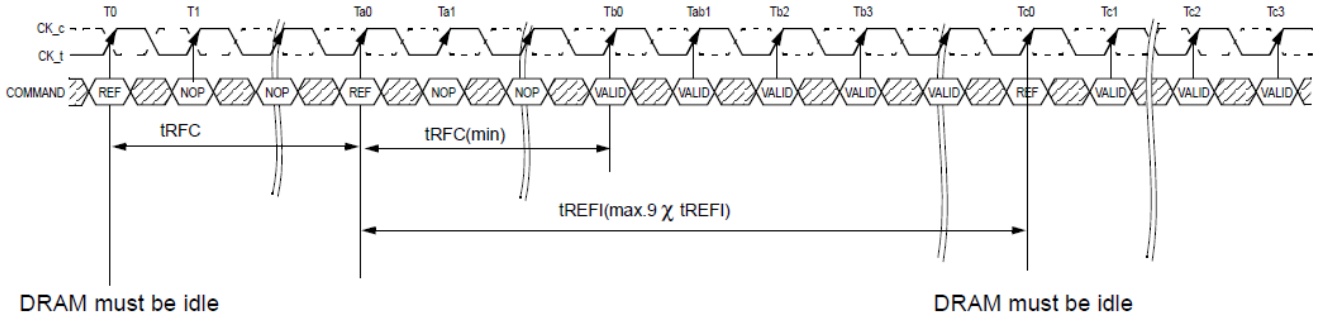
REFRESH Command Scheduling Separation Requirements

Symbol	minimum delay from	to	Notes
tRFCab	REFab	REFab	
		Activate cmd to *any* bank	
		REFpb	
tRFCpb	REFpb	REFab	
		Activate cmd to *same* bank as REFpb	
		REFpb	
tRRD	REFpb	Activate	
	ACTIVATE	REFpb affecting an idle bank (different bank than Activate)	1
		Activate cmd to *different* bank than prior Activate	
NOTE 1 A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.			

In general, an all bank refresh command needs to be issued to the LPDDR3 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in refresh command. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI. A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”) , with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8, depending on Refresh mode, Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI . At any given time, a maximum of 16 REF commands can be issued within 2 x tREFI

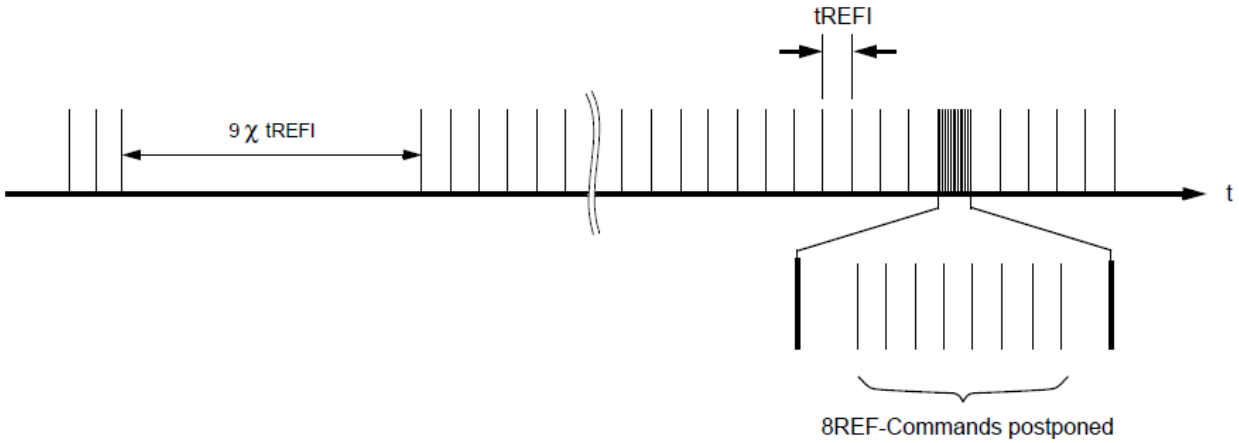
And for per bank refresh, a maximum 8 x 8 per bank refresh commands can be postponed or pulled in for scheduling efficiency. At any given time, a maximum of 2 x 8 x 8 per bank refresh commands can be issued within 2 x tREFI.

Refresh Command Timing

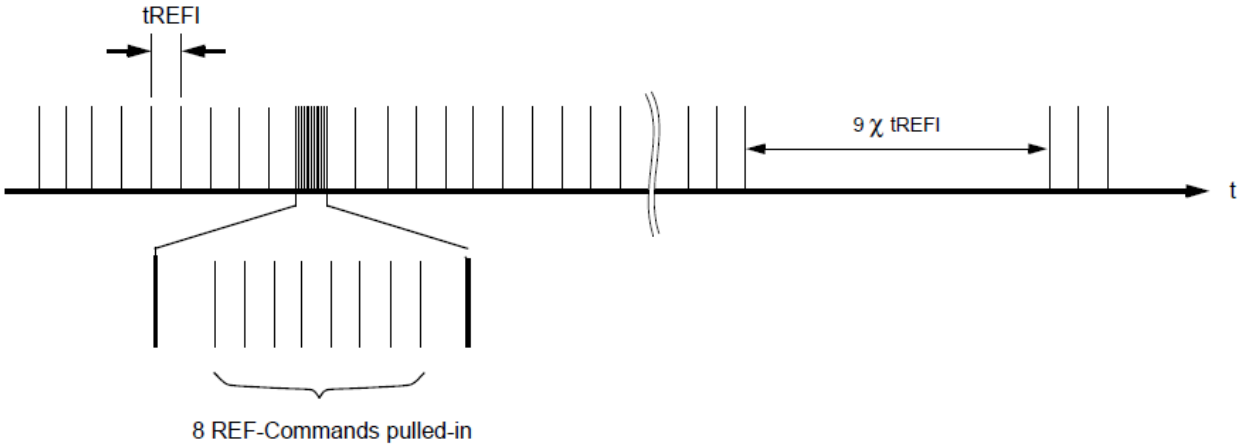


NOTE 1 Only NOP commands allowed after Refresh command registered untill tRFC(min) expires.
NOTE 2 Time interval between two Refresh commands may be extended to a maximum of 9 X tREFI.

Postponing Refresh Commands



Pulling-in Refresh Commands



REFRESH Requirements

1. Minimum number of REFRESH commands

LPDDR3 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (*t*REFW = 32 ms @ MR4[2:0] = 011 or TC ≤ 85°C). For actual values per density, and the resulting average refresh interval (*t*REFI). For *t*REFW and *t*REFI refresh multipliers at different MR4 settings.

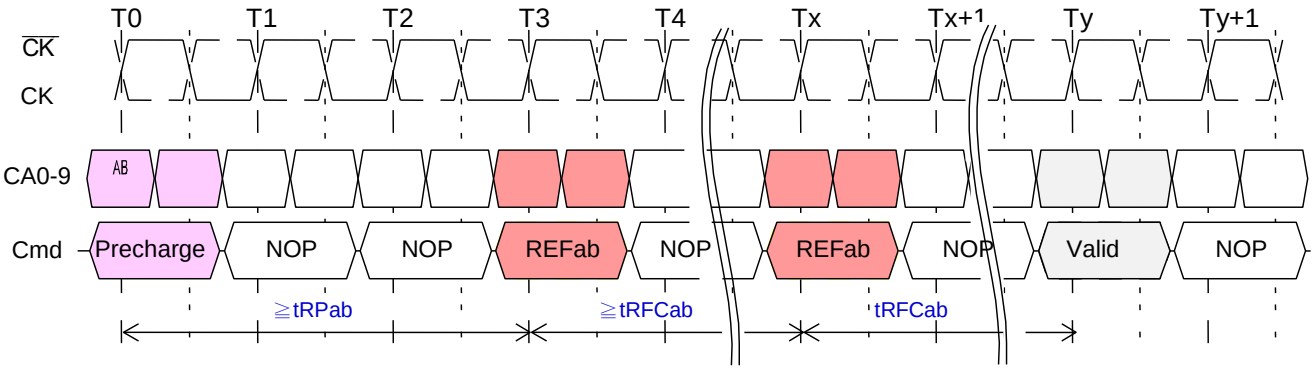
When using per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

2. REFRESH Requirements and SELF REFRESH

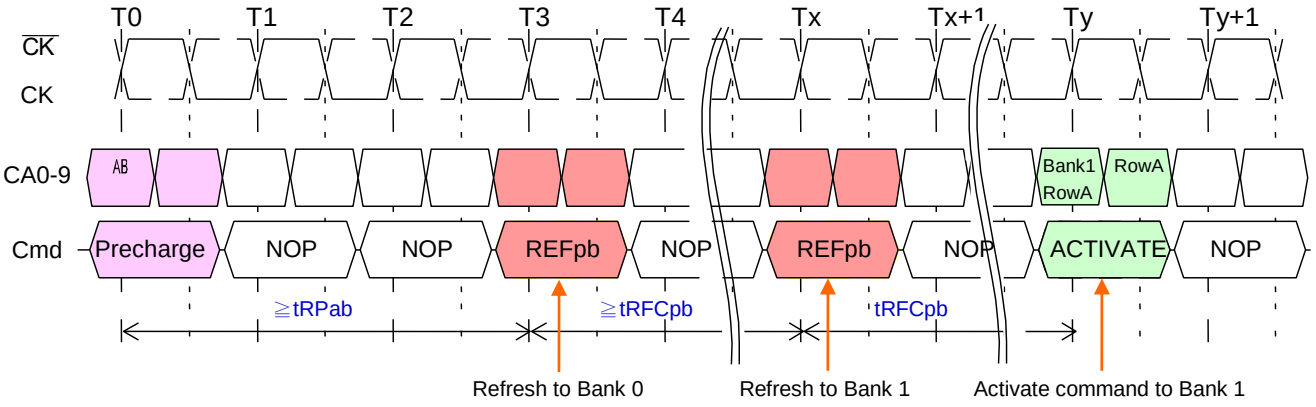
Self refresh mode may be entered with a maximum of eight refresh commands being postponed. After exiting selfrefresh mode with one or more refresh commands postponed, additional refresh commands may be postponed to the extent that the total number of postponed refresh commands (before and after the self refresh) will never exceed eight. During self-refresh mode, the number of postponed or pulled-in REF commands does not change.

“The use of self refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self refresh mode. Upon exit from self refresh, the LPDDR3 SDRAM requires a minimum of one extra refresh command before it is put back into self refresh mode.”

All-Bank REFRESH Operation



Per-Bank REFRESH Operation



NOTE 1 In the beginning of this example, the REFpb bank is pointing to bank 0.
NOTE 2 Operations to banks other than the bank being refreshed are supported during the tRFCpb period.

SELF REFRESH Operation

The SELF REFRESH command can be used to retain data in the array, even if the rest of the system is powered down. When in the self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The SELF REFRESH command is executed by taking CKE LOW, $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the clock cycle preceding a SELF REFRESH command. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are reuired after CKE is driven LOW, this timing period is defined as *t*CPDED. CKE LOW will result in deactivation of input receivers after *t*CPDED has expired. After the power-down command is registered, CKE must be held LOW to keep the device in self refresh mode.

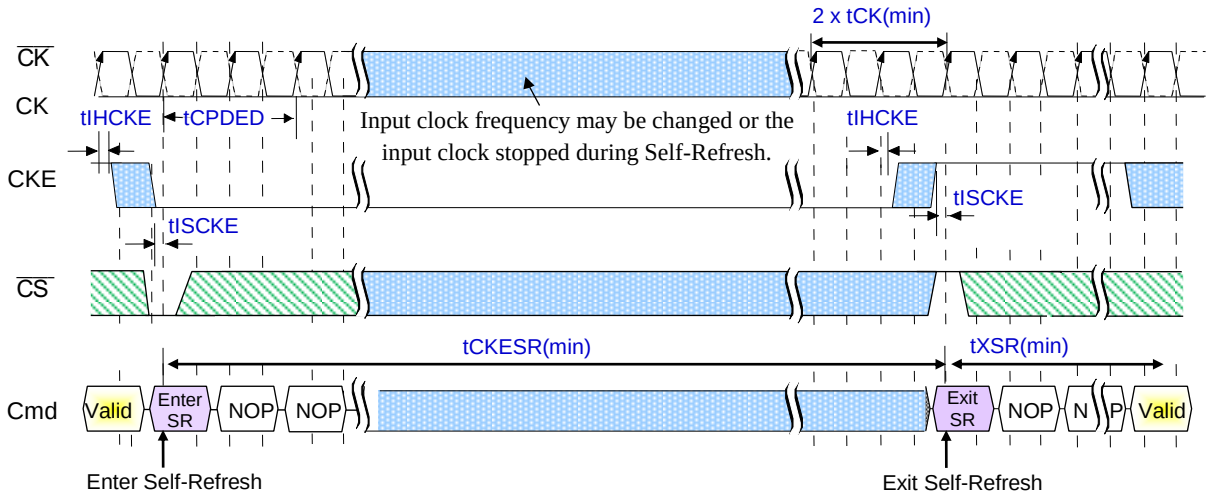
LPDDR3 devices can operate in self refresh mode in both the standard and elevated temperature ranges. These devices also manage self refresh power consumption when the operating temperature changes, resulting in the lowest possible power consumption across the operating temperature range.

Once the SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins (*V*DD1, *V*DD2, and *V*DDCA) must be at valid levels. *V*DDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, *V*DDQ must be within specified limits. *V*refDQ and *V*refCA may be at any level within minimum and maximum levels (see Absolute Maximum DC Ratings). However prior to exiting Self-Refresh, *V*refDQ and *V*refCA must be within specified limits (see Recommended DC Operating Conditions). The SDRAM initiates a minimum of one all-bank refresh command internally within *t*CKESR period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the SDRAM must remain in Self Refresh mode is *t*CKESR,min. The user may change the external clock frequency or halt the external clock tCPDED after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 *t*CK prior to the positive clock edge that registers CKE HIGH. Once Self Refresh Exit is registered, a delay of at least *t*XSR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period *t*XSR for proper operation. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval tXSR. For the description of ODT operation and specifications during self-refresh entry and exit, see section On-Die Termination.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one REFRESH command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.

Self Refresh Operation



NOTE 1 Input clock frequency can be changed or stopped during self refresh, provided that upon exiting self-refresh, a minimum of 2 cycles of stable clocks are provided, and the clock frequency is between the minimum and maximum frequencies for the particular speed grade.

NOTE 2 The device must be in the all-banks-idle state prior to entering self refresh mode.

NOTE 3 tXSR begins at the rising edge of the clock after CKE is driven HIGH.

NOTE 4 A valid command can be issued only after tXSR is satisfied. NOPs must be issued during tXSR.

Partial-Array Self Refresh: Bank Masking

LPDDR3 SDRAMs are comprised of 8 banks. Each bank can be configured independently whether a self refresh operation is taking place. One 8-bit mode register (accessible via the MRW command) is assigned to program the bankmasking status of each bank up to 8 banks.

The mask bit to the bank enables or disables a refresh operation of the entire memory space within the bank. If a bank is masked using the bank mask register, a REFRESH operation to the entire bank is blocked and bank data retention is not guaranteed in self refresh mode. To enable a REFRESH operation to a bank, the corresponding bank mask bit must be programmed as “unmasked.” When a bank mask bit is unmasked, the array space being refreshed within that bank is determined by the programmed status of the segment mask bits. bits, which is decribed in the following pages.

Partial-Array Self Refresh: Segment Masking

Programming segment mask bits is similar to programming bank mask bits. Eight segments are used for masking. A mode register is used for programming segment mask bits up to 8 bits.

When the mask bit to an address range (represented as a segment) is programmed as “masked,” a REFRESH operation to that segment is blocked. Conversely, when a segment mask bit to an address range is unmasked, refresh to that segment is enabled.

A segment-masking scheme can be used in place of or in combination with a bankmasking scheme. Each segment-mask bit setting is applied across all banks. Programming of bits in the reserved registers has no effect on the device operation.

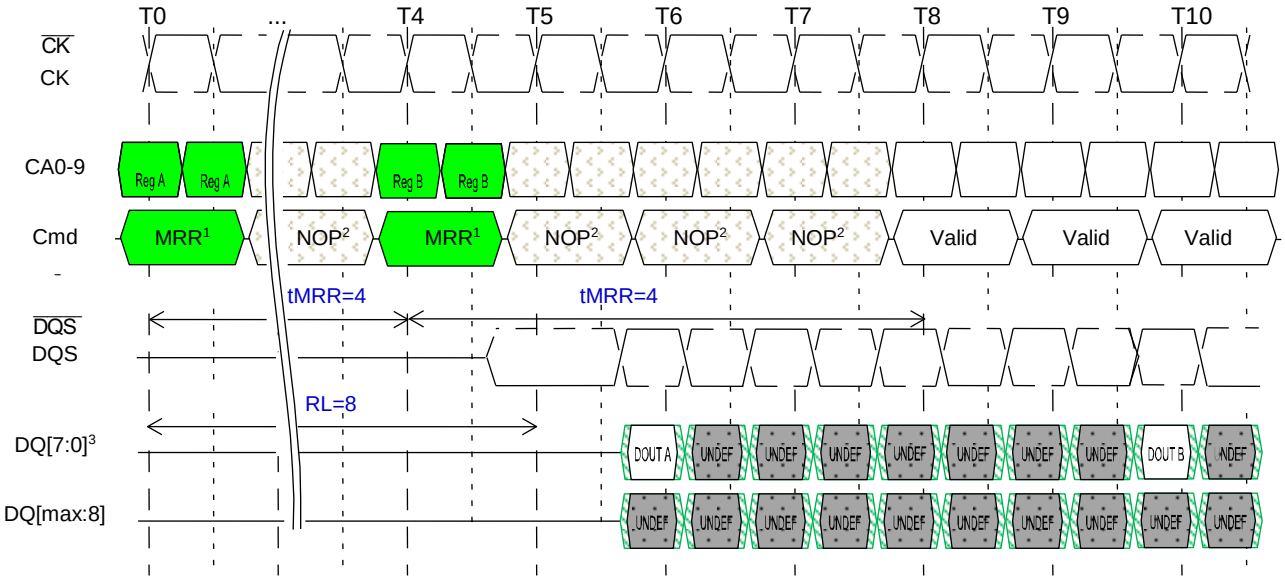
	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0		M						M
Segment 1	0		M						M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0		M						M
Segment 4	0		M						M
Segment 5	0		M						M
Segment 6	0		M						M
Segment 7	1	M	M	M	M	M	M	M	M

NOTE 1 This table illustrates an example of an 8-bank LPDDR3 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

MODE REGISTER READ (MRR)

The MRR command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f–CA0f and CA9r–CA4r. The mode register contents are available on the first data beat of DQ[7:0] after RL × *t*CK + *t*DQSCK + *t*DQSQ following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described. All DQS are toggled for the duration of the mode register READ burst.

The MRR command has a burst length of eight. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted. The MRR command period is defined as *t*MRR.



NOTE 1 MRRs to DQ calibration registers MR32 and MR40 are described in “DQ Calibration” .

NOTE 2 Only the NOP command is supported during tMRR.

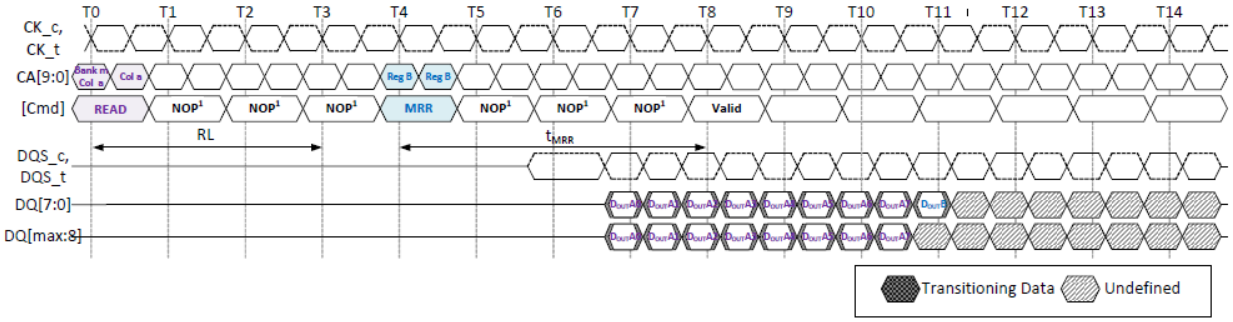
NOTE 3 Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.

NOTE 4 Minimum Mode Register Read to write latency is RL + RU(tDQSCKmax/tCK) + 8/2 + 1 - WL clock cycles.

NOTE 5 Minimum Mode Register Read to Mode Register Write latency is RL + RU(tDQSCKmax/tCK) + 8/2 + 1clock cycles.

NOTE 6 In this example, RL = 8 for illustration purposes only. After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, or WL + 1 + BL/2 + RU(tWTR/tCK) clock cycles after a prior WRITE command, as READ bursts and WRITE bursts must not be truncated by MRR.

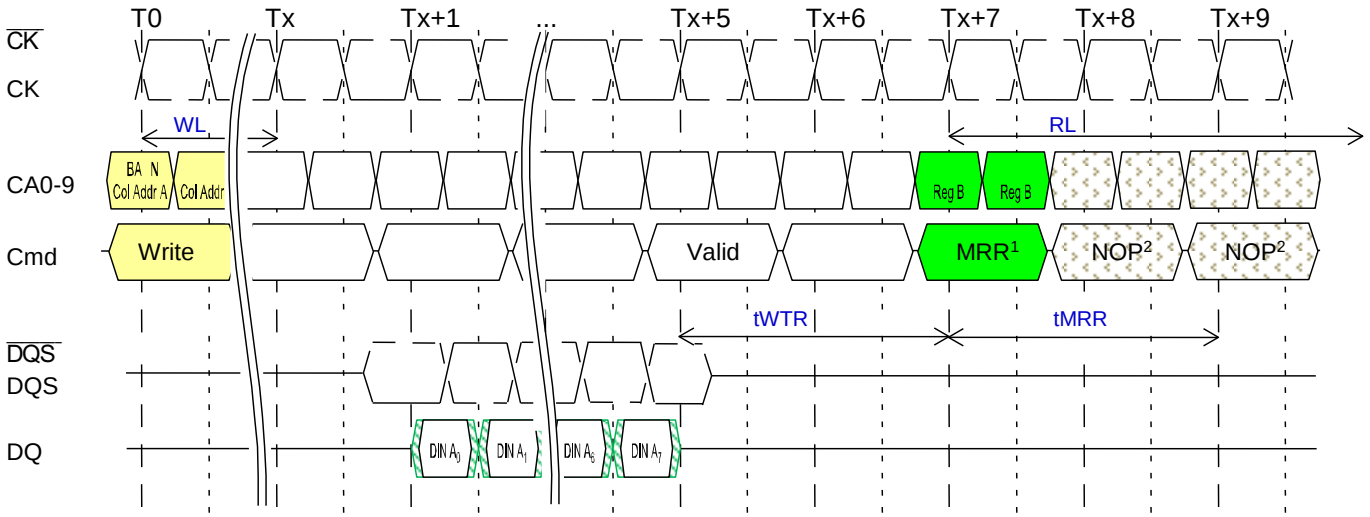
READ to MRR Timing



NOTE 1 The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
NOTE 2 Only the NOP command is supported during tMRR.

After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, or WL + 1 + BL/2 + RU(*t*WTR/*t*CK) clock cycles after a prior WRITE command, as READ bursts and WRITE bursts must not be truncated by MRR.

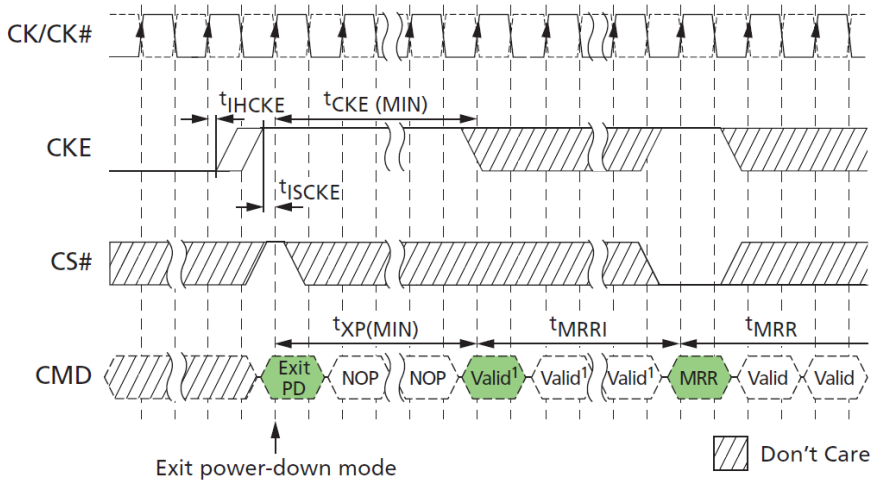
Burst WRITE Followed by MRR



NOTE 1 The minimum number of clock cycles from the burst WRITE command to the MRR command is [WL + 1 + BL/2 + RU(tWTR/tCK)].
NOTE 2 Only the NOP command is supported during tMRR.

MRR Following Idle Power-Down State

Following the idle power-down state, an additional time, *t*MRRI, is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to *t*RCD) is required in order to be able to maximize power-down current savings by allowing more power-up time fo rthe MRR data path after exit from the idle power-down state.



NOTE 1 Any valid command except MRR.

Temperature Sensor

LPDDR3 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature can be used to determine if operating temperature requirements are being met.

Temperature sensor data can be read from MR4 using the Mode Register Read protocol. Upon exiting self-refresh or power-down, the device temperature status bits will be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification that applies for the standard or extended temperature ranges. For example, TCASE could be above 85°C when MR4[2:0] equals 011B. LPDDR3 devices shall allow for 2ºC temperature margin between the point at which the device updates the MR4 value and the point at which the controller re-configures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following specifications.

Parameter	Symbol	Edge	Value	Unit	Notes
System Temperature Gradient	**TempGradient**	Max	System Dependent	ºC/s	Maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.
MR4 Read Interval	**ReadInterval**	Max	System Dependent	ms	Time period between MR4 READs from the system.
Temperature Sensor Interval	**tTSI**	Max	32	ms	Maximum delay between internal updates of MR4.
System Response Delay	**SysRespDelay**	Max	System Dependent	ms	Maximum response time from an MR4 READ to the system response.
Device Temperature Margin	**TempMargin**	Max	2	ºC	Margin above maximum temperature to support controller response.

These devices accommodate the temperature margin between the point at which the device temperature enters the elevated temperature range and point at which the controller re-configures the system accordingly. To determine the required MR4 polling frequency, the system must use the maximum TempGradient and the maximum response time of the system using the following equation:

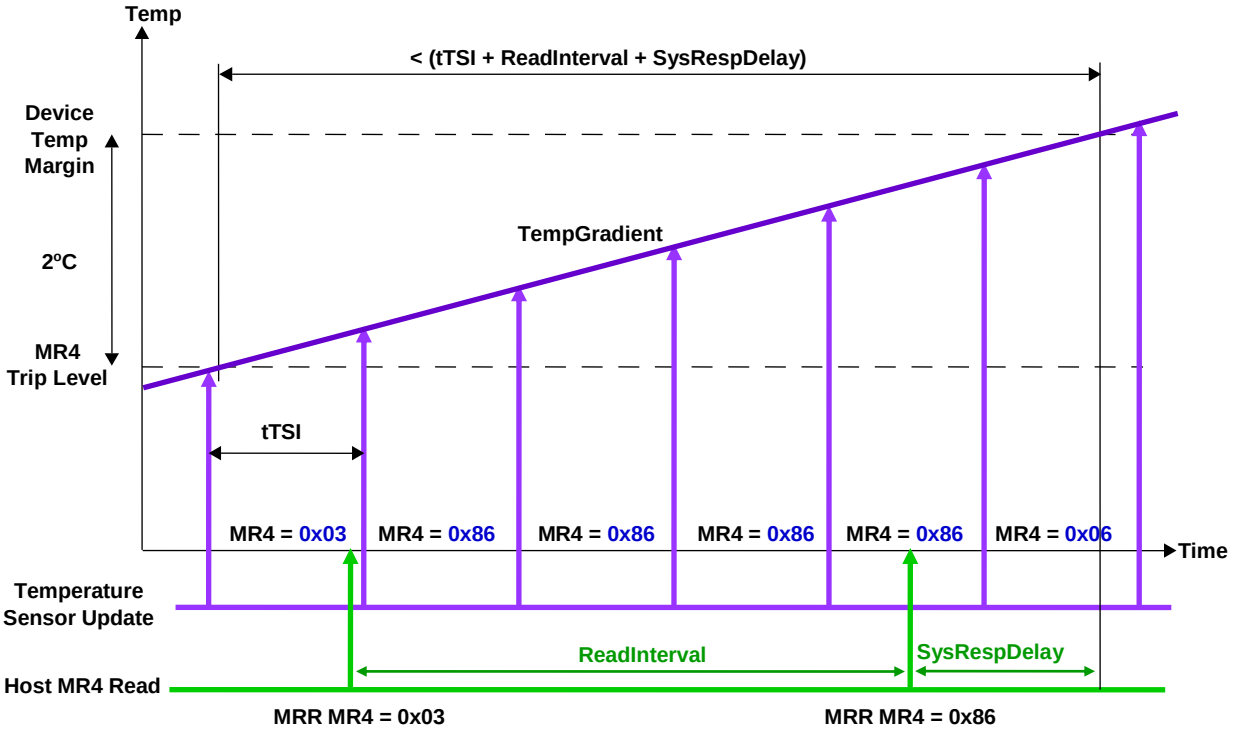
$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leqq 2°C$$

For example, if TempGradient is 10°C/s and the SysRespDelay is 1ms:

10ºC/s x (ReadInterval + 32ms + 1ms) <= 2ºC

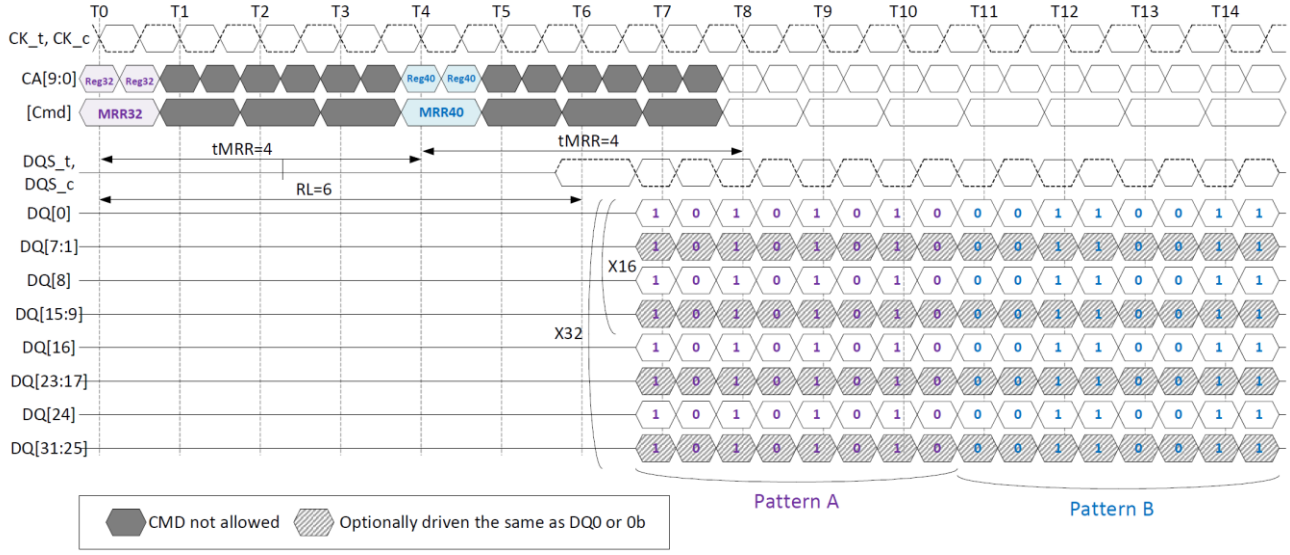
In this case, ReadInterval must not exceed 167ms.

Temperature Sensor Timing



DQ Calibration

LPDDR3 devices feature a DQ calibration function that outputs one of two predefined system-timing calibration patterns. An MRR operation to MR32 (pattern A) or an MRR operation to MR40 (pattern B) will return the specified pattern on DQ0 and DQ8; and on DQ0, DQ8, DQ16, and DQ24 for x32 devices. For x16 devices, DQ[7:1] and DQ[15:9] drive the same information as DQ0 during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] drive the same information as DQ0 during the MRR burst. MRR DQ calibration commands can occur only from the idle state.



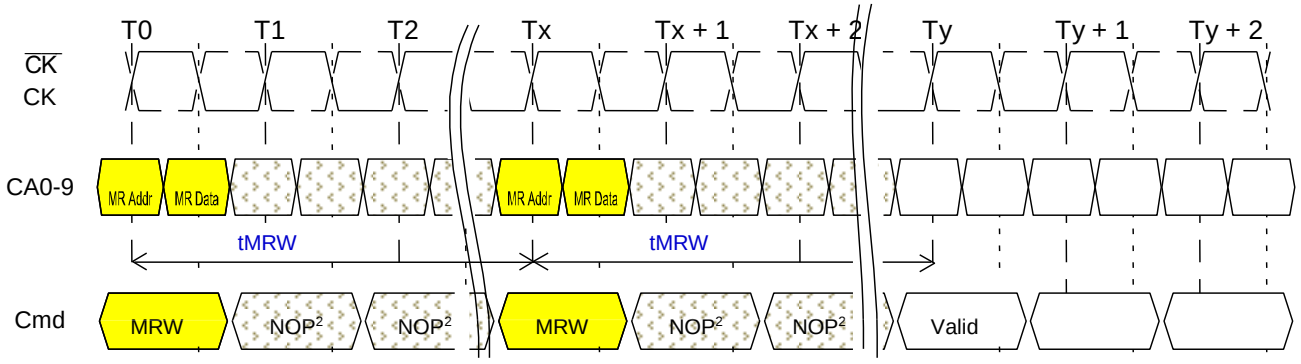
Data Calibration Pattern Description

Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Bit Time 4	Bit Time 5	Bit Time 6	Bit Time 7
Pattern A	MR32	1	0	1	0	1	0	1	0
Pattern B	MR40	0	0	1	1	0	0	1	1

Mode Register Write (MRW) Command

The Mode Register Write (MRW) command is used to write configuration data to mode registers. The MRW command is initiated with $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f-CA0f, CA9r-CA4r. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by *t*MRW. Mode register WRITEs to read-only registers have no impact on the functionality of the device.

MODE REGISTER WRITE Timing



NOTE 1 At time Ty, the device is in the idle state.
NOTE 2 Only the NOP command is supported during tMRW.

MRW

MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE-ALL command.

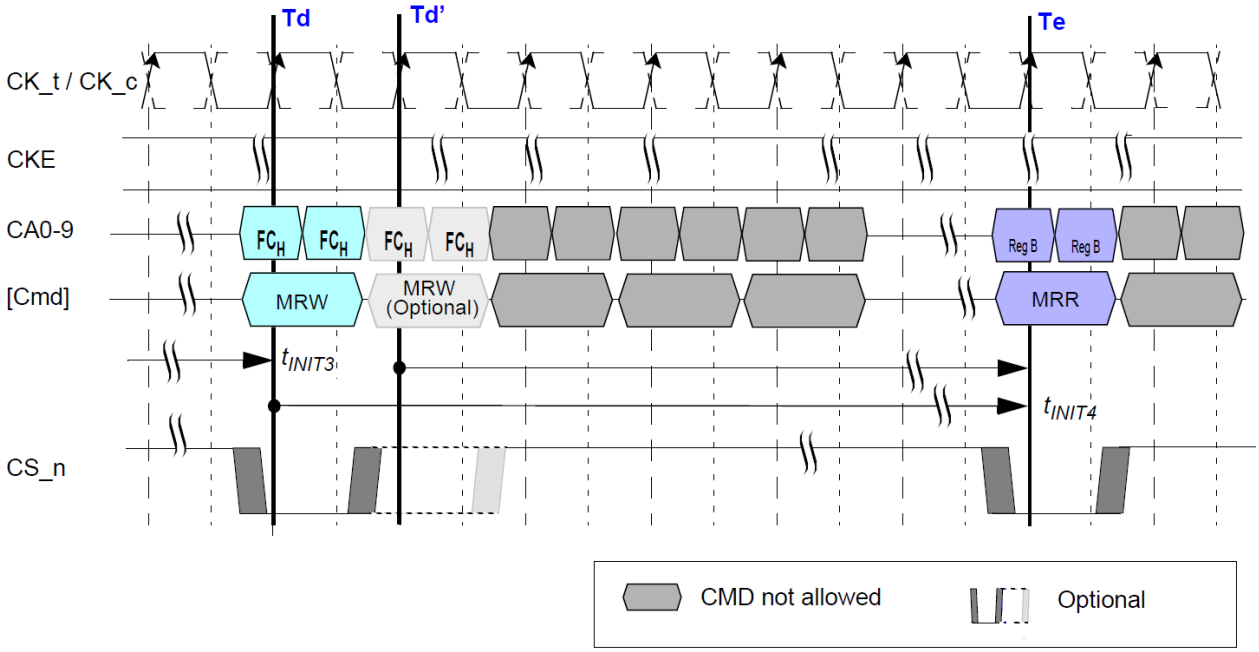
Truth Table for MRR and MRW

Current State	Command	Intermediate State	Next State
All Banks idle	MRR	Mode Register Reading (All Banks idle)	All Banks idle
	MRW	Mode Register Writing (All Banks idle)	All Banks idle
	MRW (Reset)	Restting (Device Auto-Init)	All Banks idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) idle)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (Reset)	Not Allowed	Not Allowed

Mode Register Write Reset (MRW Reset)

The MRW RESET command brings the device to the device auto-initialization (resetting) state in the power-on initialization sequence (see “Voltage Ramp and Device Initialization”). The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command.

If the initialization is to be performed at-speed (greater than the recommended boot clock frequency), then CA Training may be necessary to ensure setup and hold timings. Since the MRW RESET command is required prior to CA Training, an alternate MRW RESET command with an op-code of 0xFCh should be used. This encoding ensures that no transitions occur on the CA bus. Prior to CA Training, it is recommended to hold the CA bus stable for one cycle prior to, and one cycle after, the issuance of the MRW RESET command to ensure setup and hold timings on the CA bus.



NOTE 1 Optional MRW RESET command and optional $\overline{CS}$ assertion are allowed, When optional MRW RESET command is used, *t*INIT4 starts at Td’.

MRW ZQ Calibration Command

The MRW command is used to initiate the ZQ calibration command. This command is used to calibrate the output driver impedance across process, temperature, and voltage. LPDDR3 devices support ZQ calibration.

There are four ZQ calibration commands and related timings: tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT is for initialization calibration; tZQRESET is for resetting ZQ to the default output impedance; tZQCL is for long calibration(s); and tZQCS is for short calibration(s). See calibration command-code definitions.

The initialization ZQ calibration (ZQINIT) must be performed for LPDDR3. ZQINIT provides an output impedance accuracy of ±15 percent. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of ±15 percent. A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system.

The ZQ reset command (ZQRESET) resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQ correction) of output impedance errors within tZQCS for all speed bins, assuming the maximum sensitivities specified are met. The appropriate interval between ZQCS commands can be determined from using these tables and system-specific parameters.

LPDDR3 devices are subject to temperature drift rate (TdriftrateE) and voltage drift rate (Vdriftrate) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

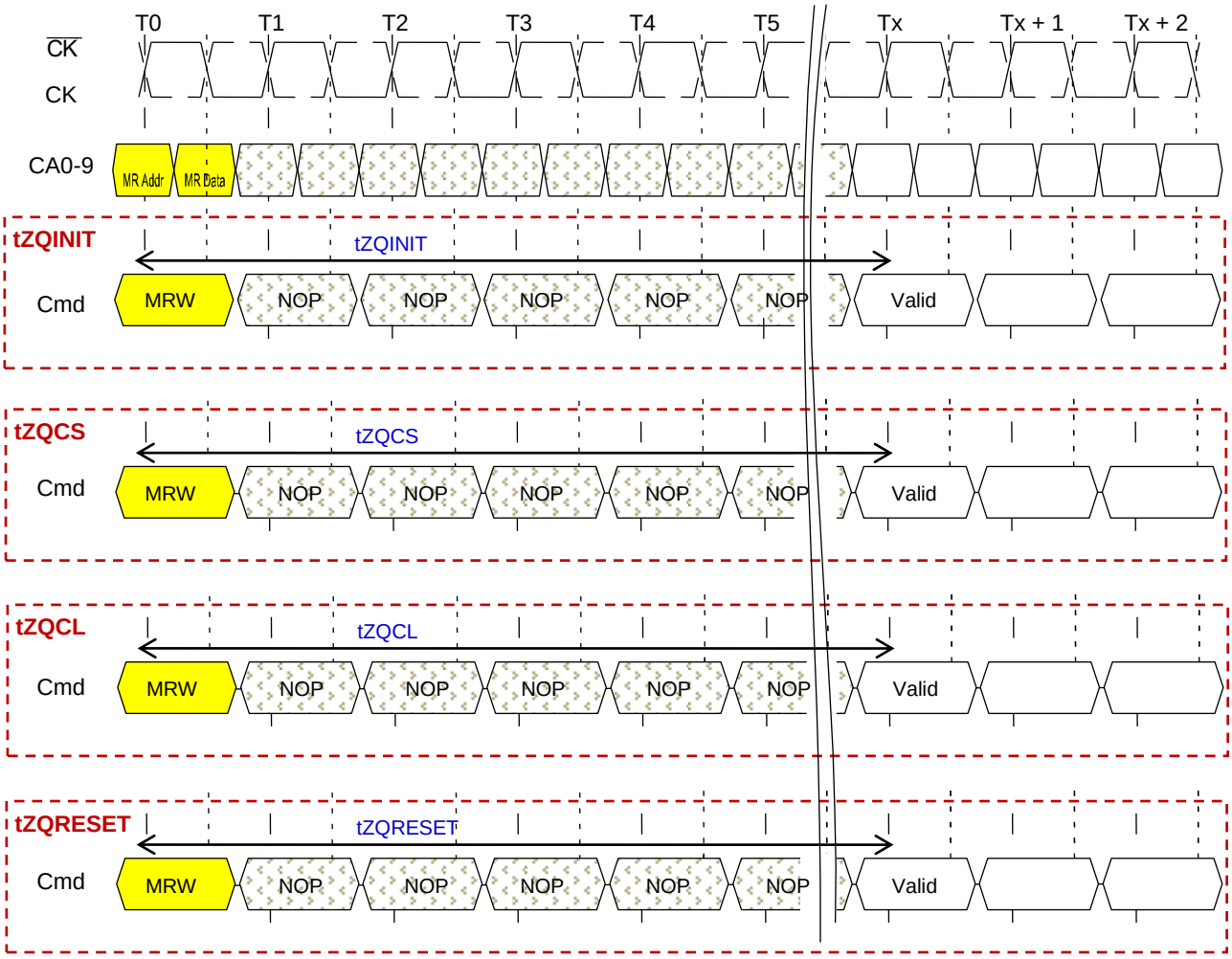
$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)} = CalibrationInterval$$

Where T_{sens} = MAX (dR_{ON}dT) and V_{sens} = MAX (dR_{ON}dV) define temperature and voltage sensitivities.
For example, if T_{sens} = 0.75%/°C, V_{sens} = 0.20%/mV, $T_{driftrate}$ = 1°C/sec, and
$V_{driftrate}$ = 15mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

A ZQ calibration command can only be issued when the device is in the idle state with all banks precharged. ODT shall be disabled via the mode register or the ODT pin prior to issuing a ZQ calibration command. No other activities can be performed on the data bus and the data bus shall be un-terminated during calibration periods (*t*ZQINIT, *t*ZQCL, or *t*ZQCS). The quiet time on the data bus helps to accurately calibrate output impedance. There is no required quiet time after the ZQ RESET command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is complete, the ZQ ball circuitry is disabled to reduce power consumption. In systems sharing a ZQ resistor between devices, the controller must prevent *t*ZQINIT, *t*ZQCS, and *t*ZQCL overlap between the devices. ZQ RESET overlap is acceptable.

ZQ Timings



NOTE 1 Only the NOP command is supported during ZQ calibration.
NOTE 2 CKE must be registered HIGH continuously during the calibration period.
NOTE 3 All devices connected to the DQ bus should be High-Z during the calibration process.

ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a R_{ZQ} ±1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited.

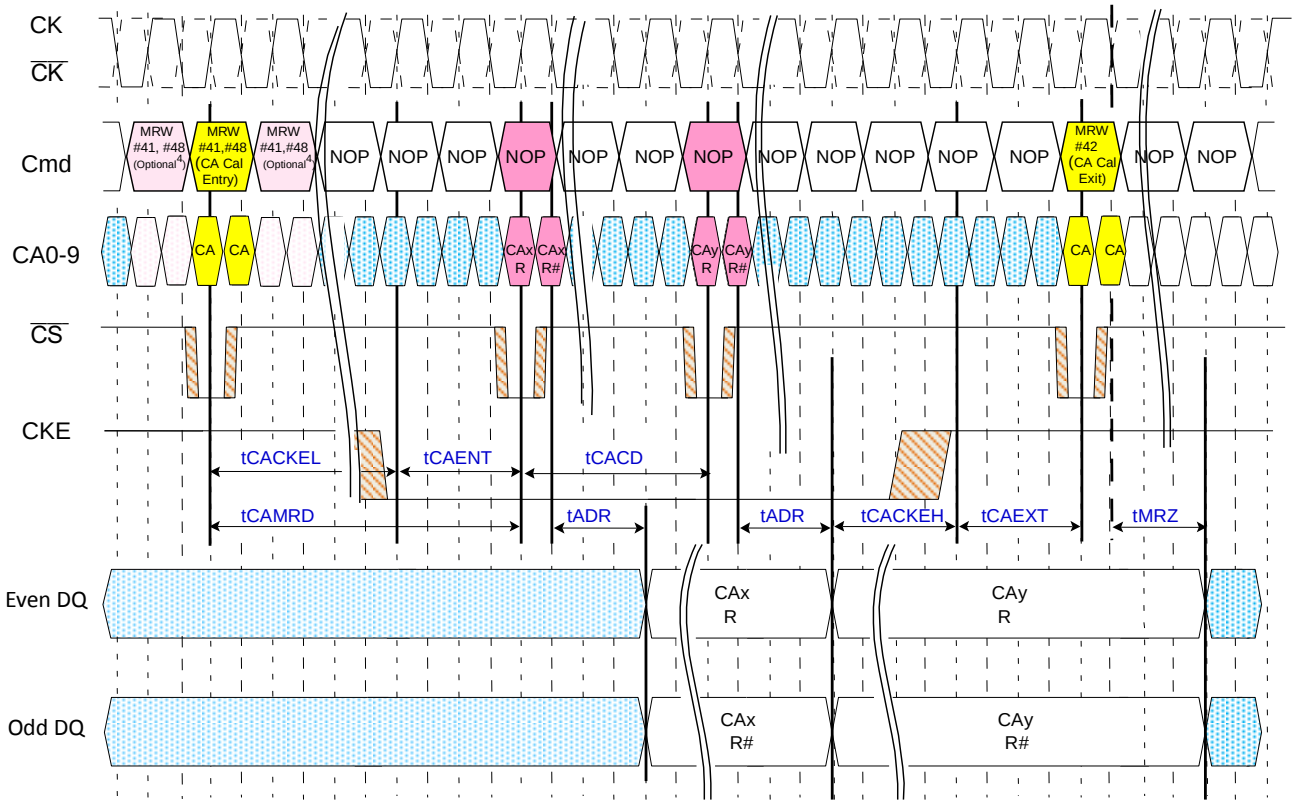
MRW - CA Training Mode

Because CA inputs operate as double data rate, it may be difficult for memory controller to satisfy CA input setup/hold timings at higher frequency. A CA Training mechanism is provided.

CA Training Sequence

1. CA Training mode entry: Mode Register Write to MR41
2. CA Training session: Calibrate CA0, CA1, CA2, CA3, CA5, CA6, CA7 and CA8
3. CA to DQ mapping change: Mode Register Write to MR48
4. Additional CA Training session: Calibrate remaining CA pins (CA4 and CA9)
5. CA Training mode exit: Mode Register Write to MR42

CA Training Timing



NOTE 1 Unused DQ must be valid HIGH or LOW during data output period. Unused DQ may transition at the same time as the active DQ. DQS must remain static and not transition.

NOTE 2 CA to DQ mapping change via MR 48 omitted here for clarity of the timing diagram. Both MR41 and MR48 training sequences must be completed before exiting the training mode (MR42). To enable a CA to DQ mapping change, CKE must be driven HIGH prior to issuance of the MRW 48 command. For details, please refer to CA Training Sequence section.

NOTE 3 Because data out control is asynchronous and will be an analog delay from when all the CA data is available, tADR and tMRZ are defined from CK falling edge.

NOTE 4 It is recommended to hold the CA bus stable for one cycle prior to and one cycle after the issuance of the MRW CA Training Entry Command to ensure setup and hold timings on the CA bus.

NOTE 5 Clock phase may be adjusted in CA training mode while $\overline{CS}$ is high and CKE is low resulting in an irregular clock with shorter/longer periods and pulse widths.

NOTE 6 Optional MRW 41, 48, 42 command and CA calibration command are allowed. To complement these optional commands, optional $\overline{CS}$ assertions are also allowed. All timing must comprehend these optional $\overline{CS}$ assertions:

a) tADR starts at the falling clock edge after the last registered $\overline{CS}$ assertion.
b) tCACD, tCACKEL, tCAMRD start with the rising clock edge of the last $\overline{CS}$ assertion.
c) tCAENT, tCAEXT need to be met by the first $\overline{CS}$ assertion.
d) tMRZ will be met after the falling clock edge following the first $\overline{CS}$ assertion with exit (MRW#42) command.

The LPDDR3 SDRAM may not properly recognize a Mode Register Write command at normal operation frequency before CA Training is finished. Special encodings are provided for CA Training mode enable/disable. MR41 and MR42 encodings are selected so that rising edge and falling edge values are the same. The LPDDR3 SDRAM will recognize MR41 and MR42 at normal operation frequency even before CA timing adjustments have been made. Calibration data will be output through DQ pins. CA to DQ mapping is described in below table.

After timing calibration with MR41 is finished, users will issue MRW to MR48 and calibrate remaining CA pins (CA4 and CA9) using (DQ0/DQ1and DQ8/DQ9) as calibration data output pins.

CA Training mode enable (MR41(29H, 0010 1001b), OP=A4H(1010 0100b))

Clock edge	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
CK rising edge	L	L	L	L	H	L	L	H	L	H
CK falling edge	L	L	L	L	H	L	L	H	L	H

CA Training mode disable (MR42(2AH,0010 1010b),OP=A8H(1010 1000b))

Clock edge	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
CK rising edge	L	L	L	L	L	H	L	H	L	H
CK falling edge	L	L	L	L	L	H	L	H	L	H

CA to DQ mapping (CA Training mode enabled with MR41)

Clock edge	CA0	CA1	CA2	CA3	CA5	CA6	CA7	CA8
CK rising edge	DQ0	DQ2	DQ4	DQ6	DQ8	DQ10	DQ12	DQ14
CK falling edge	DQ1	DQ3	DQ5	DQ7	DQ9	DQ11	DQ13	DQ15

CA Training mode enable (MR48(30H, 0011 0000b), OP=C0H(1100 0000b))

Clock edge	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
CK rising edge	L	L	L	L	L	L	L	L	H	H
CK falling edge	L	L	L	L	L	L	L	L	H	H

CA to DQ mapping (CA Training mode is enabled with MR48)

Clock edge	CA4	CA9
CK rising edge	DQ0	DQ8
CK falling edge	DQ1	DQ9

NOTE 1 Other DQs must have valid output (either HIGH or LOW).

MRW - Write Leveling Mode

In order to provide for improved signal integrity performance, the LPDDR3 SDRAM provides a write leveling feature to compensate for timing skew, affecting timing parameters such as *t*DQSS, *t*DSS, and *t*DSH.

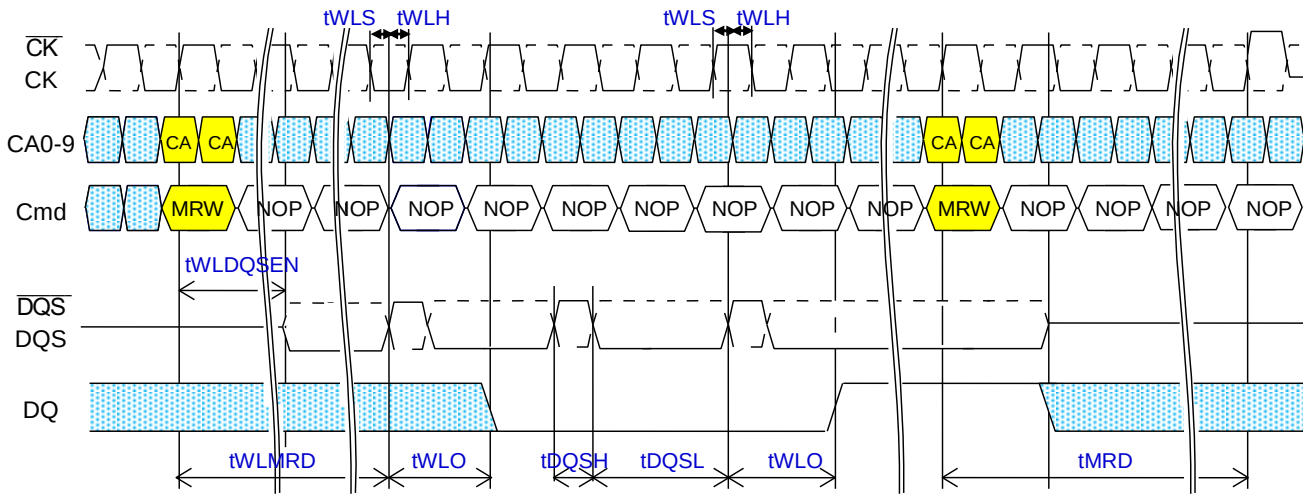
The memory controller uses the write leveling feature to receive feedback from the SDRAM allowing it to adjust the clock to data strobe signal relationship for each DQS/$\overline{\text{DQS}}$ signal pair. The memory controller performing the leveling must have adjustable delay setting on DQS/$\overline{\text{DQS}}$ signal pair to align the rising edge of DQS signals with that of the clock signal at the DRAM pin. The DRAM asynchronously feeds back CLK, sampled with the rising edge of DQS signals. The controller repeatedly delays DQS signals until a transition from 0 to 1 is detected. The DQS signals delay established through this exercise ensures the *t*DQSS specification can be met.

All data bits carry the leveling feedback to the controller (DQ[15:0] for x16 configuration, DQ[31:0] for x32 configuration). All DQS signals must be leveled independently.

The LPDDR3 SDRAM enters into write leveling mode when mode register MR2[7] is set HIGH. When entering write leveling mode, the state of the DQ pins is undefined. During write leveling mode, only NOP commands are allowed, or MRW command to exit write leveling operation. Upon completion of the write leveling operation, the DRAM exits from write leveling mode when MR2[7] is reset LOW.

The controller will drive DQS LOW and $\overline{\text{DQS}}$ HIGH after a delay of *t*WLDQSEN. After time *t*WLMRD, the controller provides DQS signal input which is used by the DRAM to sample the clock signal driven from the controller. The delay time *t*WLMRD(max) is controller dependent. The DRAM samples the clock input with the rising edge of DQS and provides asynchronous feedback on all the DQ bits after time *t*WLO. The controller samples this information and either increment or decrement the DQS and/or $\overline{\text{DQS}}$ delay settings and launches the next DQS/$\overline{\text{DQS}}$ pulse. The sample time and trigger time is controller dependent. Once the following DQ/ $\overline{\text{DQS}}$ transition is sampled, the controller locks the strobe delay settings, and write leveling is achieved for the device.

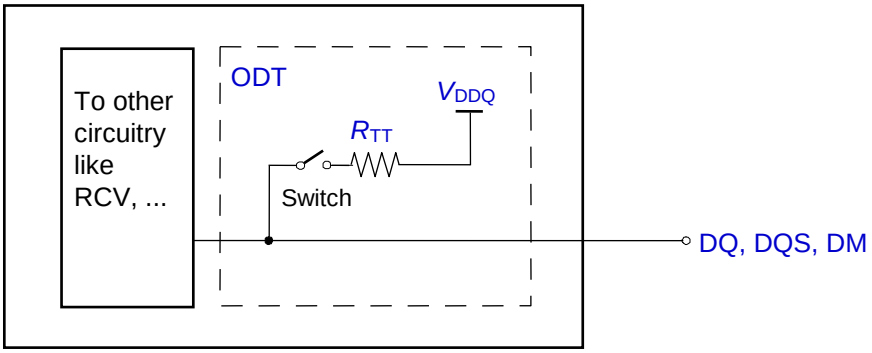
Write Leveling Timing



On-Die Termination

ODT (On-Die Termination) is a feature of the LPDDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS/$\overline{\text{DQS}}$ and DM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. The ODT pin directly controls ODT operation and is not sampled by the clock.

The ODT feature is turned off and not supported in self-refresh and deep power down modes. The DRAM will also disable termination during read operations. ODT operation can optionally be enabled during power down mode via a mode register.



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other mode register control information. The value of *R*TT is determined by the settings of mode register bits.

ODT Mode Register

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other mode register control information. The value of RTT is determined by the settings of Mode Register bits. The ODT pin will be ignored if the Mode Register MR11 is programmed to disable ODT, in self-refresh, in deep power down, in CKE power down (mode register option) and during read operations.

Asynchronous ODT

When enabled, the ODT feature is controlled asynchronously based on the status of the ODT pin. ODT is off under any of the following conditions:

– ODT is disabled through MR11[1:0]
– DRAM is performing a read operation (RD or MRR)
– DRAM is in power down mode and MR11[2] is zero
– DRAM is in self-refresh or deep power down modes.
– DRAM is in CA Training Mode.

In asynchronous ODT mode, the following timing parameters apply when ODT operation is controlled by the ODT pin: *t*ODToff,min,max, *t*ODTon,min,max.

Minimum *R*TT turn-on time (*t*ODTon,min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum *R*TT turn on time (*t*ODTon,max) is the point in time when the ODT resistance is fully on. *t*ODTon,min and *t*ODTon,max are measured from ODT pin high.

Minimum *R*TT turn-off time (*t*ODToff,min) is the point in time when the device termination circuit starts to turn off the ODT

resistance. Maximum ODT turn off time (*t*ODToff,max) is the point in time when the on-die termination has reached high impedance. *t*ODToff,min and *t*ODToff,max are measured from ODT pin low.

ODT During Read Operations (RD or MRR)

During read operations, LPDDR3 SDRAM will disable termination and disable ODT control through the ODT pin. After read operations are completed, ODT control is resumed through the ODT pin (if ODT mode is enabled).

ODT During Power Down

When MR11 OP<2> is zero, termination control through the ODT pin will be disabled when the DRAM enters CKE power down. After a power down command is registered, termination will be disabled within a time window specified by tODTd,min,max. After a power down exit command is registered, termination will be enabled within a time window specified by tODTe,min,max.

Minimum RTT disable time (tODTd,min) is the point in time when the device termination circuit is no longer be controlled by the ODT pin. Maximum ODT disable time (tODTd,max) is the point in time when the on-die termination will be in high impedance.

Minimum RTT enable time (tODTe,min) is the point in time when the device termination circuit will no longer be in high impedance. The ODT pin shall control the device termination circuit after maximum ODT enable time

(tODTe,max) is satisfied. When MR11[2] is enabled and MR11[1:0] are non zero, ODT operation is supported during CKE power down with ODT control through the ODT pin.

ODT During Self Refresh

LPDDR3 SDRAM disables the ODT function during self refresh. After a self refresh command is registered, termination will be disabled within a time window specified by tODTd,min,max. After a self refresh exit command is registered, termination will be enabled within a time window specified by tODTe,min,max.

ODT During Deep Power Down

LPDDR3 SDRAM disables the ODT function during deep power down. After a deep power down command is registered, termination will be disabled within a time window specified by *t*ODTd,min,max.

ODT During CA Training and Write Leveling

During CA Training Mode, LPDDR3 SDRAM will disable on-die termination and ignore the state of the ODT control pin. For ODT operation during Write Leveling mode, refer to below table for termination activation and deactivation for DQ and DQS/$\overline{\text{DQS}}$. If ODT is enabled, the ODT pin must be high, in Write Leveling mode.

DRAM Termination Function in Write Leveling Mode

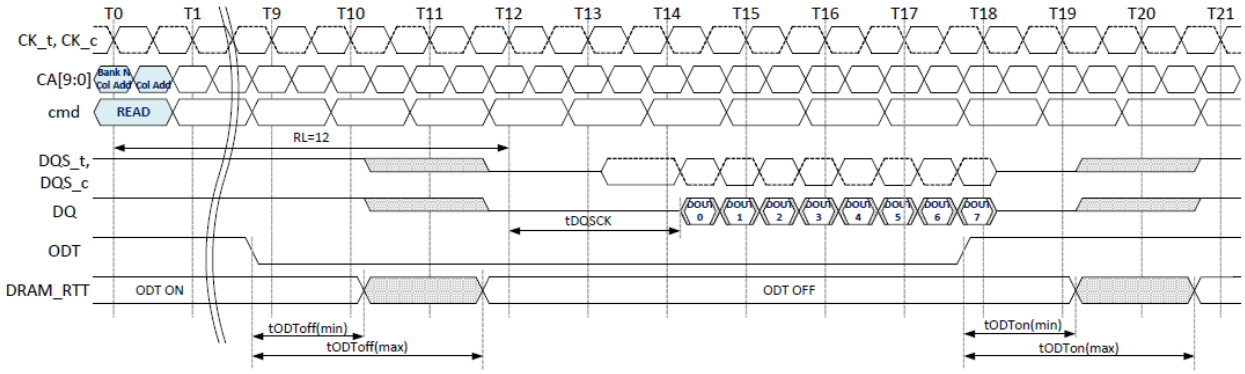
ODT pin	DQS/$\overline{DQS}$ termination	DQ termination
de-asserted	OFF	OFF
asserted	ON	OFF

ODT States Truth Table

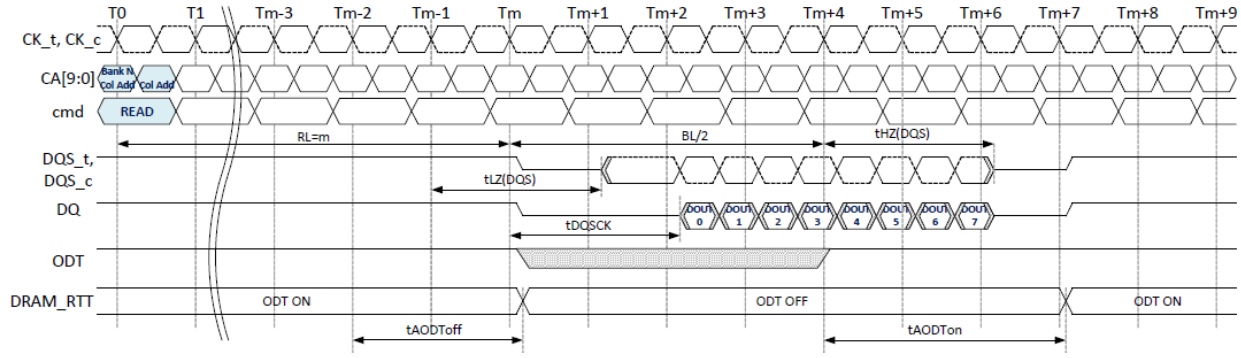
	Write	Read/DQ Cal	ZQ Cal	CA Training	Write Level
DQ Termination	Enabled	Disabled	Disabled	Disabled	Disabled
DQS Termination	Enabled	Disabled	Disabled	Disabled	Enabled

NOTE 1 ODT is enabled with MR11[1:0]=01b, 10b, or 11b and ODT pin HIGH. ODT is disabled with MR11[1:0]=00b or ODT pin LOW.

Asynchronous ODT Timing Example for RL = 12

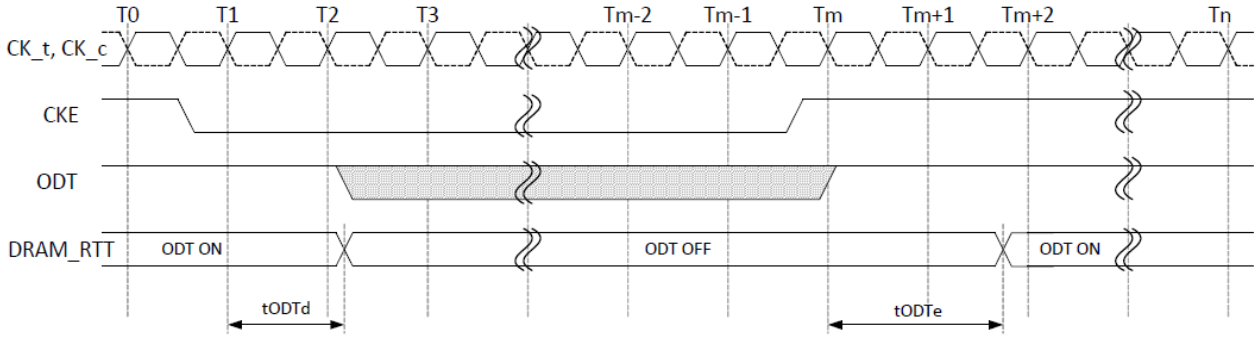


Automatic ODT Timing During READ Operation Example for RL = *m*



NOTE 1 The automatic RTT turn-off delay, tAODToff, is referenced from the rising edge of "RL-2" clock at Tm-2.
NOTE 2 The automatic RTT turn-on delay, tAODTon, is referenced from the rising edge of "RL+ BL/2" clock at Tm+4

ODT Timing During Power Down, Self Refresh, Deep Power Down Entry/Exit Example



NOTE 1 Upon exit of Deep Power Down mode, a complete power-up initialization sequence is required.

Power-Down

Power-down is entered synchronously when CKE is registered LOW and $\overline{CS}$ is HIGH at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as row activation, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down *I*DD specification will not be applied until such operations are complete.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, and CKE. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as *t*CPDED. CKE LOW will result in deactivation of input receivers after *t*CPDED has expired. In power-down mode, CKE must be held LOW; all other input signals are “Don’t Care.” CKE LOW must be maintained until *t*CKE is satisfied. *V*REFCA must be maintained at a valid level during power-down.

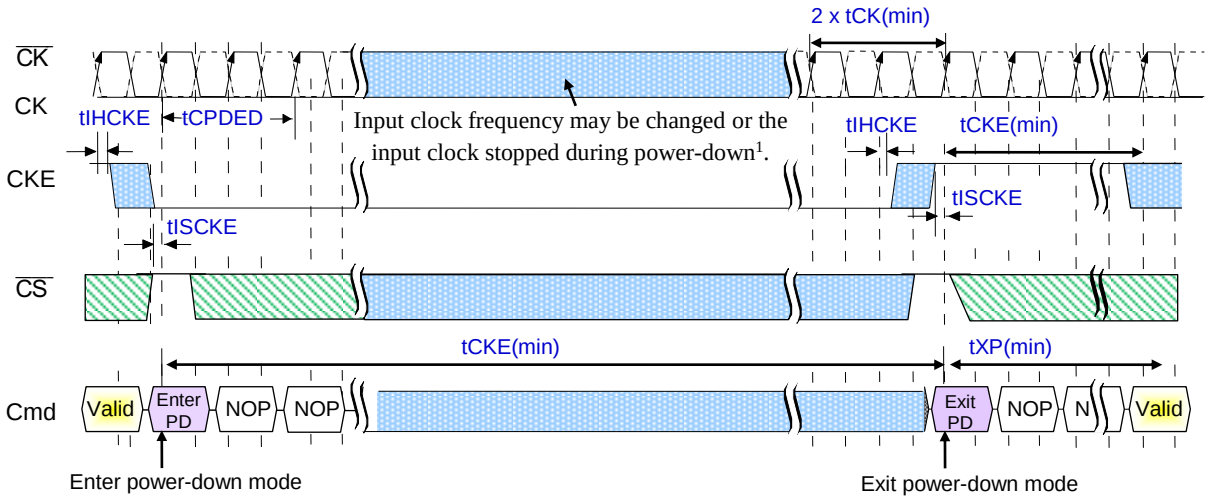
*V*DDQ can be turned off during power-down. If *V*DDQ is turned off, *V*REFDQ must also be turned off. Prior to exiting power-down, both *V*DDQ and *V*REFDQ must be within their respective minimum/maximum operating ranges.

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in section “REFRESH Command”.

The power-down state is exited when CKE is registered HIGH. The controller must drive $\overline{CS}$ HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE,min is satisfied. A valid, executable command can be applied with power-down exit latency *t*XP after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.

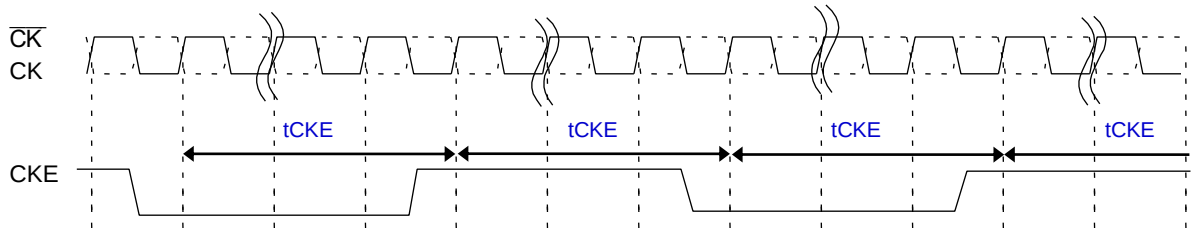
If power-down occurs when all banks are idle, this mode is referred to as idle powerdown; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Basic Power-Down Entry and Exit Timing

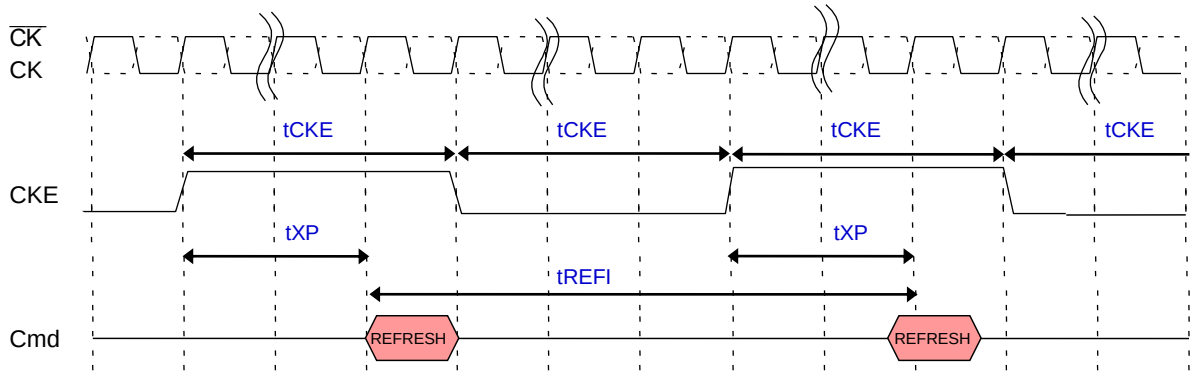


NOTE 1 Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

CKE-Intensive Environment

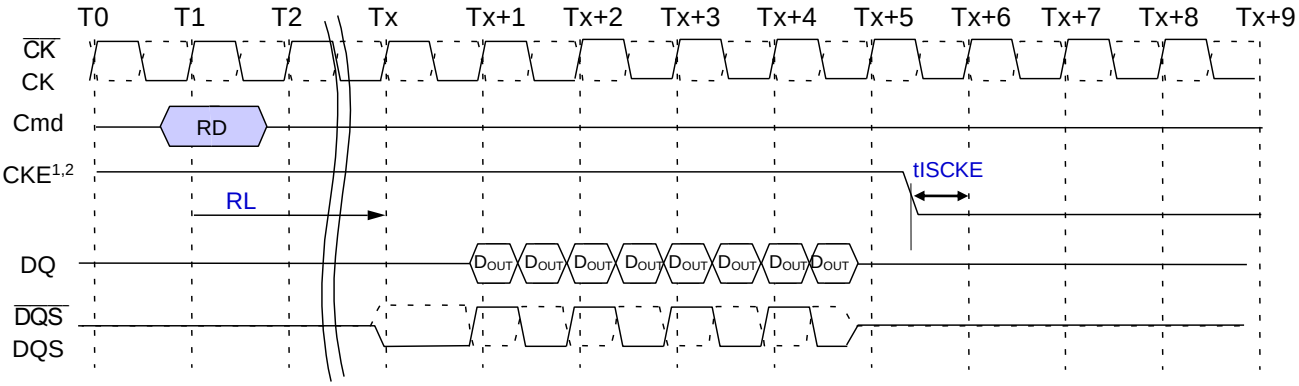


REFRESH-to-REFRESH Timing in CKE-Intensive Environments



NOTE 1 The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

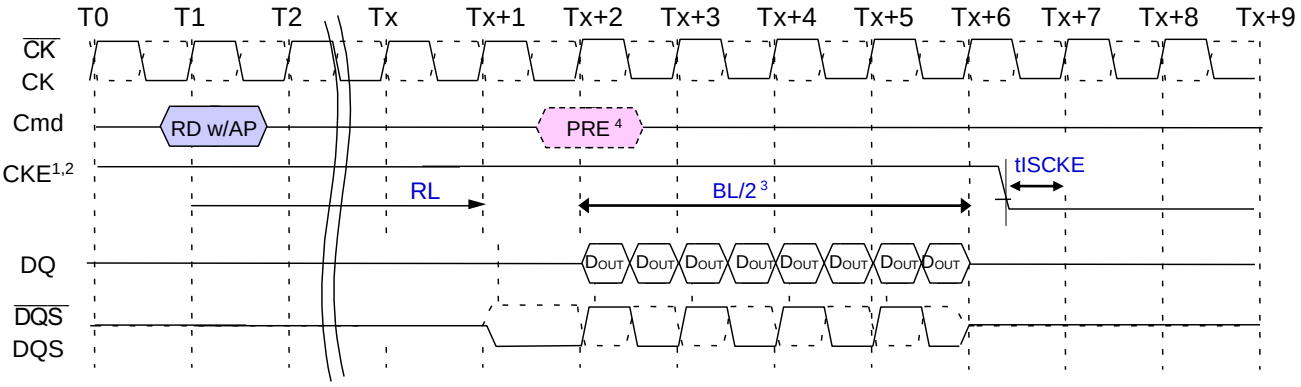
READ to Power-Down Entry



NOTE 1 CKE must be held HIGH until the end of the burst operation.

NOTE 2 CKE can be registered LOW at RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 clock cycles after the clock on which the READ command is registered.

READ with Auto Precharge to Power-Down Entry



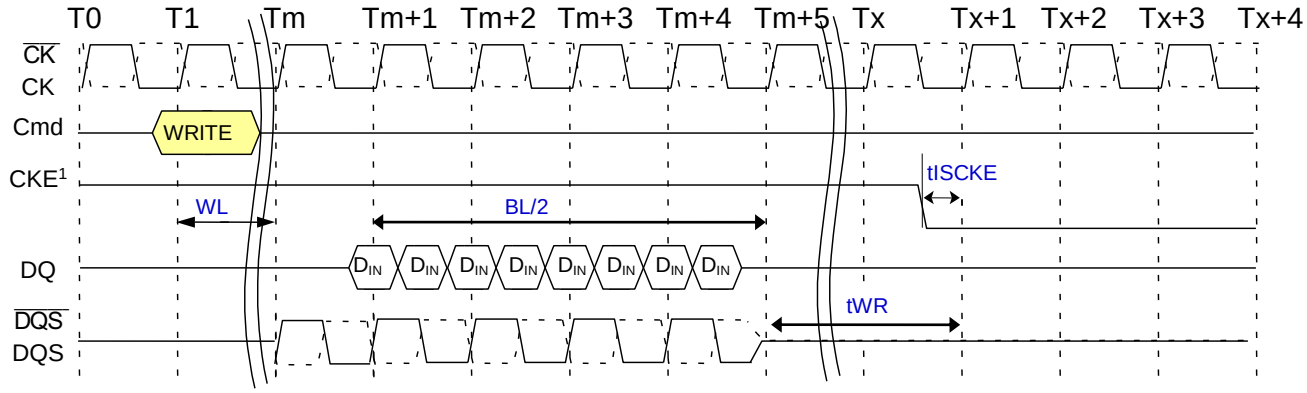
NOTE 1 CKE must be held HIGH until the end of the burst operation.

NOTE 2 CKE can be registered LOW at RL + RU(tDQSCK/tCK)+ BL/2 + 1 clock cycles after the clock on which the READ command is registered.

NOTE 3 BL/2 with tRTP = 7.5ns and tRAS (MIN) is satisfied.

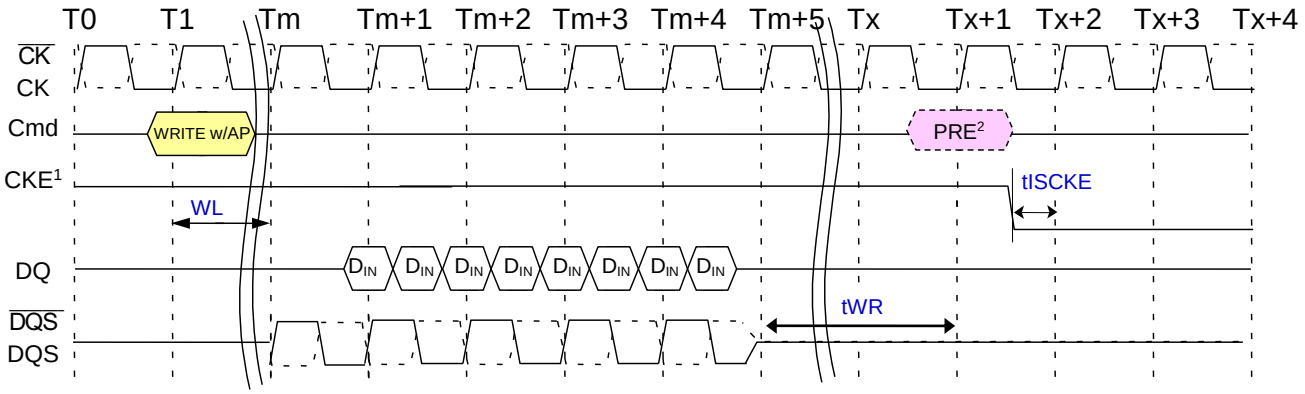
NOTE 4 Start internal PRECHARGE.

WRITE to Power-Down Entry



NOTE 1 CKE can be registered LOW at WL + 1 + BL/2 + RU(tWR/tCK) clock cycles after the clock on which the WRITE command is registered.

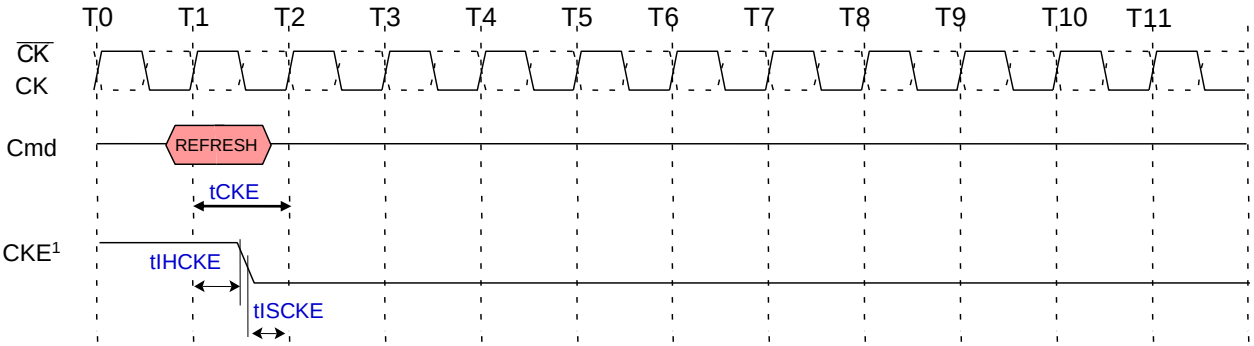
WRITE with Auto Precharge to Power-Down Entry



NOTE 1 CKE can be registered LOW at WL + 1 + BL/2 + RU(tWR/tCK) + 1 clock cycles after the WRITE command is registered.

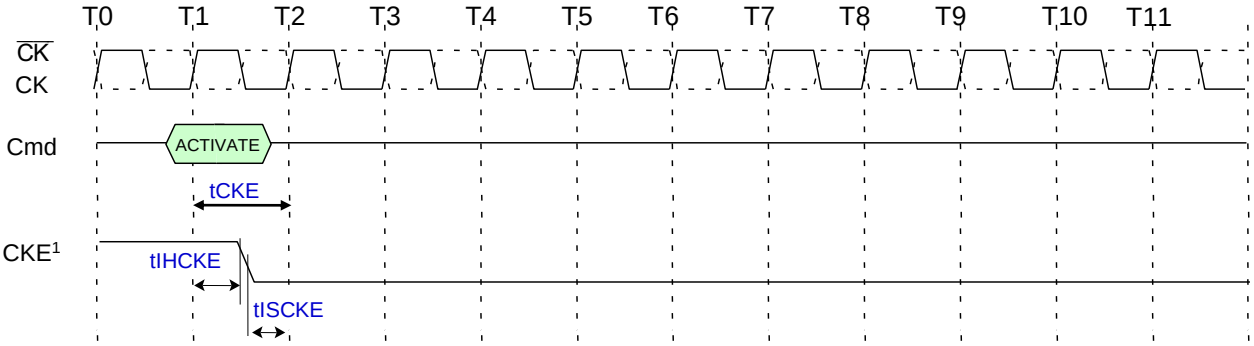
NOTE 2 Start internal PRECHARGE.

REFRESH Command to Power-Down Entry



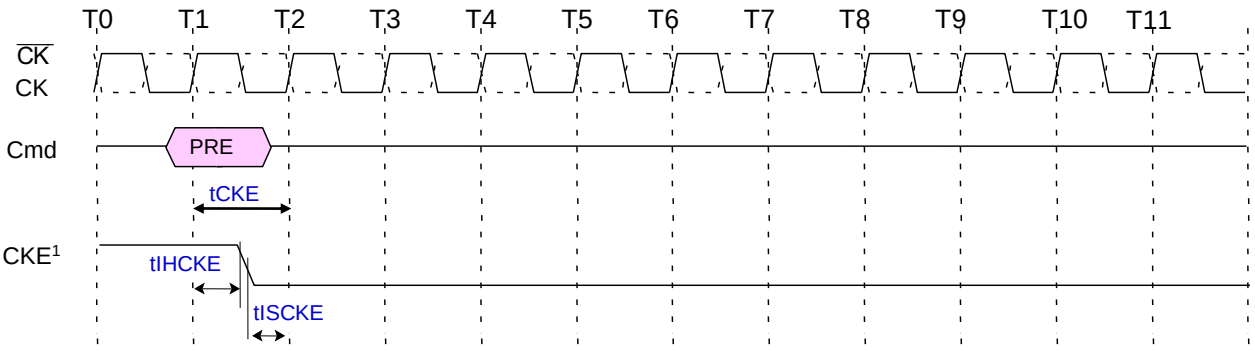
NOTE 1 CKE can go LOW tIHCKE after the clock on which the REFRESH command is registered.

ACTIVATE Command to Power-Down Entry



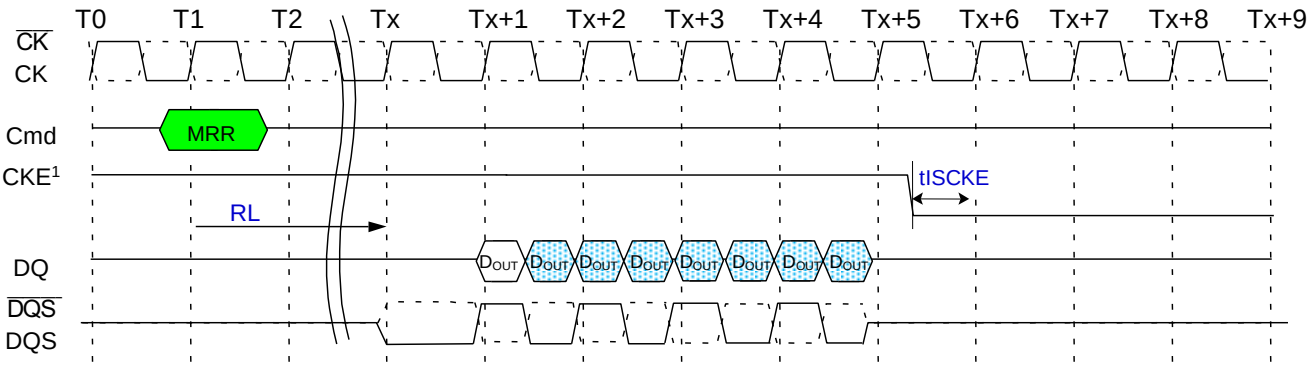
NOTE 1 CKE can go LOW tIHCKE after the clock on which the ACTIVATE command is registered.

PRECHARGE Command to Power-Down Entry



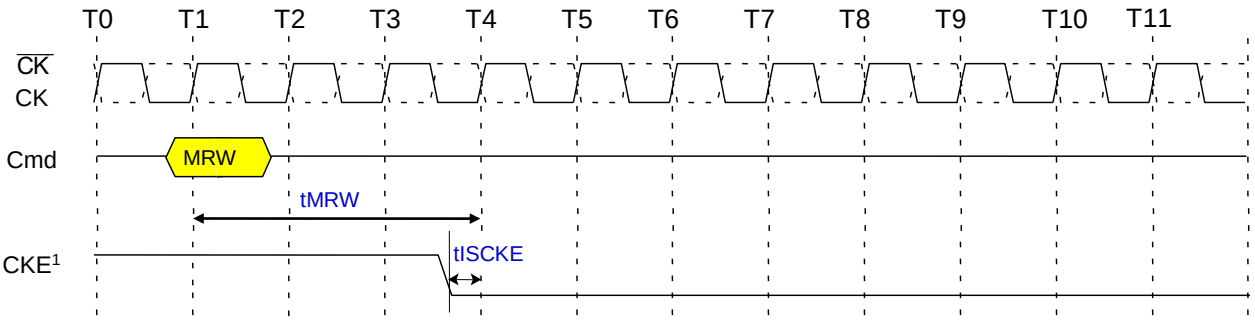
NOTE 1 CKE can go LOW tIHCKE after the clock on which the PRECHARGE command is registered.

MRR to Power-Down Entry



NOTE 1 CKE can be registered LOW RL + RU(tDQSCK/tCK)+ BL/2 + 1 clock cycles after the clock on which the MRR command is registered.

MRW to Power-Down Entry



NOTE 1 CKE can be registered LOW tMRW after the clock on which the MRW command is registered.

Deep Power-Down (DPD)

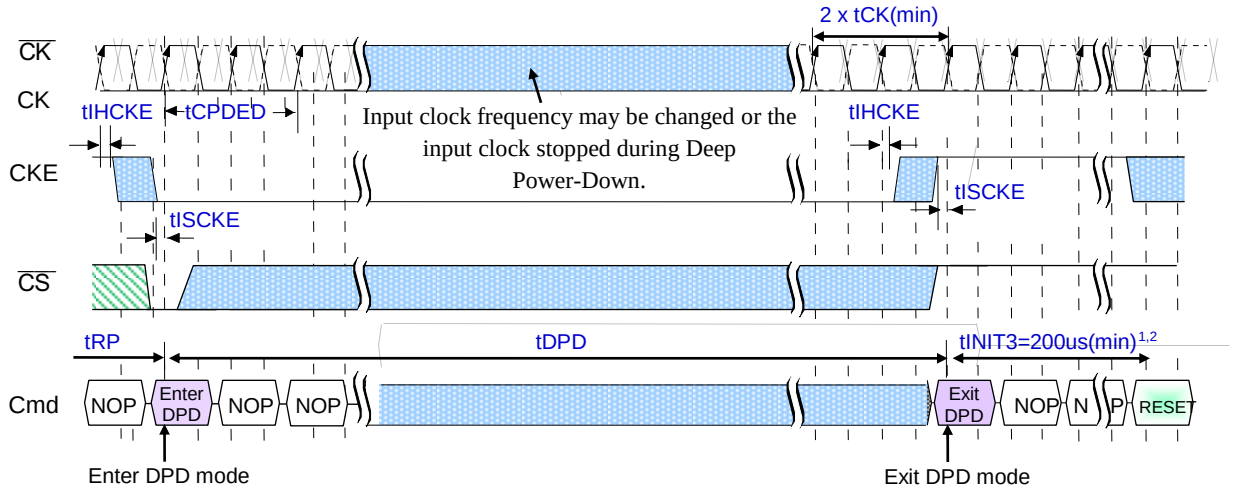
Deep power-down (DPD) is entered when CKE is registered LOW with $\overline{CS}$ LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of the clock. All banks must be in the idle state with no activity on the data bus prior to entering the DPD mode. During DPD, CKE must be held LOW. The contents of the SDRAM will be lost upon entry into DPD mode.

In DPD mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry are disabled within the device. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as tCPDED.

CKE LOW will result in deactivation of command and address receivers after tCPDED has expired. *V*REFDQ can be at any level between 0 and *V*DDQ, and *V*REFCA can be at any level between 0 and *V*DDCA during DPD. All power supplies, including *V*REF, must be within the specified limits prior to exiting DPD (see “AC and DC Operating Conditions”).

DPD mode is exited when CKE is registered HIGH, while meeting *t*ISCKE, and the clock must be stable. The device must be fully re-initialized using the power-up initialization sequence. The SDRAM is ready for normal operation after the initialization sequence is completed. For the description of ODT operation and specifications during DPD entry and exit, see “ODT During Deep Power Down”.

Deep Power-Down Entry and Exit Timing



NOTE 1 The initialization sequence can start at any time after Tx + 1.

NOTE 2 tINIT3 and Tx + 1 and refer to timings in the initialization sequence.

NOTE 3 Input clock frequency may be changed or the input clock can be stopped or floated during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Input Clock Frequency Changes and Clock Stop Events

The device supports input clock frequency change during CKE LOW under the following conditions:

- *t*CK(abs)min is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (*t*RCD, *t*RP) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies *t*CH(abs) and *t*CL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

The device supports clock stop during CKE LOW under the following conditions:

- CK is held LOW and $\overline{CK}$ is held HIGH or both are floated during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (tRCD, tRP) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.

The device supports input clock frequency change during CKE HIGH under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to changing the frequency;
- $\overline{CS}$ shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR3 SDRAM is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2*tCK + tXP.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR3 devices support clock stop during CKE HIGH under the following conditions:

- CK is held LOW and $\overline{CK}$ is held HIGH during clock stop;
- $\overline{CS}$ shall be held HIGH during clock clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to stopping the clock;
- The LPDDR3 SDRAM is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of 2*tCK + tXP.

NO OPERATION (NOP) Command

The purpose of the NOP command is to prevent the device from registering any unwanted commands issued between operations. A NOP command can only be issued at clock cycle*n* when the CKE level is constant for clock cycle N-1 and clock cycle N. A NOP command has two possible encodings:

1. $\overline{CS}$ HIGH at the clock rising edge N.
2. $\overline{CS}$ LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The NOP command will not terminate a previous operation that is still in process, such as a burst READ or WRITE cycle.

Revision History

Version	Page	Modified	Description	Released
1.0	All	-	Preliminary Release	02/2018
1.1	P1,36,67	-	Revise temperature range to -30ºC~105ºC	03/2018

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